Silicon Hybrid Wafer Scale Integration (WSI) Used to Fabricate a Hilbert Transform Integrated Circuit Module

THESIS

Daniel J. Gaughan, Captain, USAF

AFIT/GE/ENG/90D-22

DEPARTMENT OF THE AIR FORCE
AIR UNIVERSITY
AIR FORCE INSTITUTE OF TECHNOLOGY
Wright-Patterson Air Force Base, Ohio

AFIT/GE/ENG/90D-22

Silicon Hybrid Wafer Scale Integration (WSI) Used to Fabricate a Hilbert Transform Integrated Circuit Module

THESIS

Daniel J. Gaughan, Captain, USAF

AFIT/GE/ENG/90D-22

AFIT/GE/ENG/90D-22

Silicon Hybrid Wafer Scale Integration (WSI) Used to Fabricate a Hilbert Transform Integrated Circuit Module

Presented to the Faculty of the School of Engineering of the
Air Force Institute of Technology
Air University
In Partial Fulfillment of the Requirements for the Degree of
Master of Science in Electrical Engineering

THESIS
Daniel J. Gaughan, Captain, USAF

December 1990

Preface

This research was intended to fabricate a wafer-scale circuit using an improved process. While the process still needs to be perfected, the wafer-scale project at AFIT still demonstrates the potential of this technology. I had hopes of completing the process and successfully testing the device but this was not possible.

I would like to thank the people who did make this work as successful as possible. The first of whom is my advisor, Captain Mark Mehalic. Without his support I would not have completed the project. I would also like to thank the members of my committee for their comments and suggestions throughout the process.

Since I knew very little about the design of circuitry prior to this effort, I am indebted to Mr. Russell Milliron of the VLSI laboratory for his version of the non-wafer-scale Hilbert transform. I also wish to thank Captain Tom Jenkins and Mr. Dave Via of the Electronics Technology Laboratory for their help in maskmaking.

And most of all, I wish to thank my wife, Cindy and my children, Nicole and Timothy for being there for me when I needed them, even though I couldn't spend much time for them.

Table of Contents

List of Figures

Figure Page

Abstract

This research was performed in order to develop a superior processing schedule for fabricating Wafer-Scale Integration (WSI) circuit modules. This technology allows the design of circuitry that spans the entire surface of a silicon substrate wafer. The circuit element employed in this research was the Hilbert transform, a digital phase-shifting circuit. The transform was incorporated into a three Integrated Circuit (IC) die package that consisted of a mechanically supportive silicon wafer, the three IC die, and a planarizing silicon wafer. The die were epoxied into this wafer using a Teflon block as a flat, and the combination was epoxied onto the substrate wafer, forming the IC module.

The original design goals of this research were to keep the IC die and wafer planar and to electrically characterize the module's interconnects. The first goal was met; the resultant process uses a low temperature (50^{o}C) cure to achieve die-to-wafer planarity of within 5 microns. The second was not met due to the inability to pattern the chosen photosensitive dielectric material.

Recommendations for further research included the need to use a stable non-stick surface as a epoxy cure fixture and the need to investigate the photopatternable dielectric material.

SILICON HYBRID WAFER SCALE INTEGRATION (WSI) USED TO FABRICATE A HILBERT TRANSFORM INTEGRATED CIRCUIT MODULE.

I. Introduction

Background

Wafer Scale integration (WSI) combines discrete integrated circuit elements on a common substrate material, and it incorporates the interconnections required to form a single functional circuit module by using the surface area and bulk of an entire semiconductor wafer which serves a a host substrate. The WSI practice has two main implementation methods, monolithic and hybrid. The monolithic approach begins with the conventional silicon (Si) wafer substrate, and integrated circuits (ICs) are fabricated in the usual manner, with the exception that multiple types of ICs are fabricated on the substrate and are interconnected to realize a specific circuit module. On the other hand, hybrid wafer scale integration uses integrated circuit die which have been independantly fabricated using the normal processes; these IC die are then mounted in/on another supporting material and interconnected to form the desired circuit module.

Each of these approaches posesses an associated set of problems. One of the most significant problems associated with the monolithic process is the yield of the "die." Since the monolithic approach never cuts the die out of the host wafer, each die that has a defect remains a physical part of the overall circuit module. There must be provisions made for redundant die on the wafer to ensure that a sufficient number of die survive the IC processing scheme and are capable of functioning in the circuit. The hybrid WSI option does not have

this problem since the die are cut from a wafer fabricated with a normal IC processing scheme, and the die can be physically and electrically evaluated prior to insertion into the WSI module. Most descrete IC die defects are caused prior to this step, and thus, hybrid WSI significantly overcomes the problem of inactive die.

Another problem associated with both versions of the WSI technology is the issue of interconnections. Emphasis on the interconnection especially applies to the hybrid WSI since the die are cut and mounted in a different host substrate. This situation is usually the cause of interconnection failure. For this reason, interconnection yield is most important for hybrid wafer scale integration.

Problem Statement

Previous researchers at AFIT have experienced interconnection failure due to the non-planarity of the surface at the die-to-wafer transition. The purpose of this research is to develop the methodology and materials required to produce high-yield interconnections suitable for the fabrication of wafer scale integrated circuits using the AFIT WSI design technique.

Scope

This research continues the research accomplished by previous AFIT thesis students. This research particularly focuses on the discontinuity of the junction between a mounted MOSIS fabricated IC die and the host silicon substrate's surface. The WSI module will be processed using the techniques developed at AFIT by prior researchers with the incorporation of new elements intended to improve the planarization of the wafer-to-die transition

region. The final WSI circuit module will be developed, and when complete, will be electrically characterized to evaluate the performance of the interconnection junctions.

Assumptions

1. The Si WSI processing materials evaluated in the previous research at AFIT will be used where the experimental evidence supports the superior performance of these materials. Specifically, three inch n-type silicon wafers of (100) orientation will be used as the substrate material, and sputtered aluminum will serve as the interconnecting metal. Selectilux HTR 3-200, a photoensitive polyimide, will be used as the planarizing dielectric layer material. In addition, the Master Bond EP34CA (Special) epoxy will be used to attach the discrete IC die to the Si wafer substrate. Finally, Shipley 111s positive photoresist will be used to pattern the sputtered aluminum thin films to form the needed interconnections as demonstrated by Takahashi. [1:126].

2. Only two interconnecting metalization levels will be required to fabricate the desired WSI module. Thus, no more than two interconnection levels will be investigated. This is compatible with current circuit design practice, and thus it should apply equally to this investigation.

3. The materials and processing equipment required will be available for the applicable portions of the research. While some of the equipment and materials may be substituted, certain processing equipment is essential to the performance of this investigation. In unusual circumstances the laboratories at Wright-Patterson may be able to support some limited research effort and may have resources available in the event of an equipment failure. The

equipment at AFIT has been analyzed and it is anticipated to be available and suitable to perform this research.

4. The basic WSI fabrication process investigated by previous AFIT researchers will be used to initiate this project. Refinements to the process are the focus of this work. The basic WSI fabrication methodology, as reported by Takahashi, was primarily successful [1]. The focus of this research is intended to improve the fabrication process associated with planarizing the inter-die gap region so as to relize a higher interconnection yield, not to invent a new process.

Approach

This research will begin with the design and fabrication of an IC circuit which can be used to demonstrate this wafer scale integration project. This circuit will be tested in a packaged form, and the results will be used to verify the operation in the WSI circuit. Next, optical flats of Teflon® (Tetrafluoroethylene), which will form the surface that will support the Si wafer substrate and mounted IC circuit die during the epoxy cure phase will be fabricated. The Teflon® flats will be optically examined for flatness prior to beginning the work with the wafers. The flats will be machined as flat as possible and then abrasively polished on a slurry table to achieve a higher degree of smoothness.

The Teflon® flats will be used to support and planarly align the contacting surfaces of the circuit die and silicon wafer while the epoxy cures. The circuit die will be designed using the Very Large Scale Integration (VLSI) design tools available in the AFIT VLSI facility and the MOS Implementation Service (MOSIS) fabrication program will be used to

produce the IC die. The discrete IC will be developed using normal procedures by using the MAGIC design tool available in the VLSI design facility. The circuit will have one feature not normally found on VLSI circuits developed at AFIT. This feature will consist of a ring of metal and dielectric which surrounds the perimeter of the entire IC die. This feature will ensure that the die will lie flat and that no epoxy will migrate to the surface of the IC die and thus will remain in the die-to-substrate gap.

This gap will be filled with epoxy while the die and substrate are in the face down position on the optical flat. The entire unit will be heated from below to vent any epoxy cure vapor out the back side of the host substrate surface and thus preserve the planar surface at the gap junction.

The planarizing dielectric and aluminum metal interconnection layers will then be patterned in the usual manner for discrete die-level circuits. This overall processing scheme should produce a functional circuit module on a wafer-scale level which will then be tested and electrically characterized compared to other techniques employed to produce similar devices.

Presentation

The material that follows will fully document the efforts of this research and present conclusions and recommendations for further research. Chapter II will begin with a brief review of the general area of wafer scale integration as it is discussed in the recent literature. This review will establish a departure point for this research. Chapter III will define more specifically, the procedures followed to process the wafers and the equipment used to

perform this processing. Chapter IV will present the detailed results of this research. The final chapter will make conclusions based on these results and make recommendations for any processing changes or material selection modifications required to further the research of this area.

II. Literature Review

Introduction

The approaches to wafer scale integration (WSI) are numerous. In the forward to the 1988 Electronics Components Conference, John W. Balde and John M. Segelken describe the numerous solutions to the problems of wafer scale integration. They describe tradeoffs of size, weight, speed and cost, and the promises that wafer scale integration may bring [2 :161]. They state that there are many ways to bring about the realization of wafer scale integration, and that projection is supported by the numerous and diverse methods discussed at the conference. This emphasis on WSI technology was echoed by Michael J. Little in the proceedings of the 1990 International Conference on Wafer Scale Integration [3:vii]. The following chapter will outline the significant methods that relate to this research effort.

Since this research continues the work of other researchers at AFIT, it is worthwhile to revisit some of the literature that the previous researchers have analyzed. Any differences found in the more recent literature will also be included to broaden the information presented, and update it to the present state of the research.

Metalization

To begin, the process of multilevel interconnect techniques will be reviewed. As reported by Takahashi, the planarization of successive levels of metalization becomes increasingly important [1:7]. For the two level structure proposed in this research, the metal that crosses the boundary between the IC die and the Si wafer host substrate is critical to the formation of successful metalization interconnects. Takahashi reports that all of the re-

searchers reviewed selected aluminum or aluminum alloys as the metal of choice for the interconnects [1:8]. While the current research indicates the same metal as a general trend, at least one research group is working with copper conductor lines which are electroplated to form an interconnection layer [4:1213-1223].

The research team headed by R. Wayne Johnson used sputtered aluminum for the second-level metalizationalong with conventional wet chemical etching to pattern the connections [5:845-849]. This is evidently still the preferred method since it was confirmed in a recent publication of their continuing research work [6:185-193]. This is by no means accepted as the only method of metalization patterning. As previously reported by Takahashi, the research at Rensselaer Polytechnic Institute uses a lift-off technique to achieve this requirement. The same publication also describes new research concerning techniques for depositing of the metal using ion beams, and new techniques for repairing improperly fabricated lines [7:195-205]. Most of these methods are useful only for high volume work or large industrial processors, due to the costs involved. However, the lift off technique may still be applied on small scale projects.

Dielectrics

Between the metal interconnect layers is a dielectric layer used to separate the signal lines. Several properties of good dielectrics useful in WSI technologies have been described by previous researchers [1:9]. The primary perfomance goal of the dielectric is to provide electrical insulation. It must also be able to withstand the subsequent processing steps required to fabricate the WSI circuit. Generally, the aluminum layer limits the processing

temperature to 250 ^{o}C. Many materials are used for interlevel dielectrics, but usually SiO_2 is used as the primary or base level dielectric. The interlevel dielectrics are varied, and they span the polyimides to the resins which have a low cure temperature and good dielectric properties. This dielectric "...served the dual function of smoothing the surface topology and passivating the chip surface " [1:189]. The choice of an interlevel dielectric must be matched with that of the die attach material, and this was made clear by researchers from Auburn University who state ..."It is necessary to chose a material whose cure process, i.e., temperature, is compatable with the temperature limits of the epoxy." [5:848] and also "... the brittle glass layer over the less rigid epoxy can result in the fracture of the glass during subsequent thermal exposures." [6:189]

R. F. McDonald from the Center for Integrated Electronics at Renssalaer discusses some of the problems involved with WSI and describes the thermal stress of materials used in WSI circuits and warns against shrinkage and the importance of matching the thermal coefficient of expansion (TCE) of the substrate materials [7:197-198]. John Hagge discusses other important aspects of the substrate in his discussion of silicon-on-silicon packaging. He states that the advantages of using silicon as a substrate are numerous. Some of which are: TCE match with many VLSI die, active devices may be manufactured as a part of the substrate, wafers compatable with current chip processing techniques, a low cost ("less than $1 per square inch"), and a flat stable platform for incorporating the IC die [8:171].

As for the installation process, there is diversity here too. Some of the hybrid work uses the flip-chip technology; here the chip is placed face down onto the surface of the

substrate and attached to it by means of solder bumps [9:180]. Other techniques attach the IC die to the surface in the face-up position and use wire bonding to electrically connect the chip and the substrate [8:172].

Summary

The previous sections show that research continues in the area of wafer scale integration. The progress made by various researchers has established that advancements are being made in the techniques and material choices. No significant changes have been made since the initial studies by AFIT researchers and their recommendations remain valid. The basic process that has been decided upon for WSI at AFIT remains one of the leading methods for achieving WSI.

III. Equipment and Experimental Procedure

The following chapter describes the physical structure of the WSI project and the methods selected to create the structure. Each of the components will be described, and the rationale for the selection will be given. The IC circuit die design, the substrate and its preparation, the epoxy and its application, and the metalization and its design and application will be expiained.

IC Circuit Design

The first objective was to design the die-level IC. The circuit chosen for this research was the Hilbert transform. This circuit is intended to be part of the DRFM (Digital Radio Frequency Memory) project currently being designed at AFIT. The Hilbert transform performs a phase shift of a digitized input waveform. The circuit was modified from a non-wafer scale version to enable intermediate results. The mathematical function of the transform is shown in the Figure 1. The circuit was designed using the MAGIC software tool which is in the VLSI Laboratory at AFIT. A schematic of this circuit is shown in Figure 2, and a description follows.

$$y(n-5) = 19/32\ [\ x(n-6)\ -\ x(n-4)] + 4/32\ [\ x(n-8) - x(n-2)] + 1/32\ [x(n-10) - x(n)]$$

Where x(n) is current data,
x(n-2) is data from two clock cycles previous, etc.
y(n) is transform output

Figure 1. Hilbert transform equation.

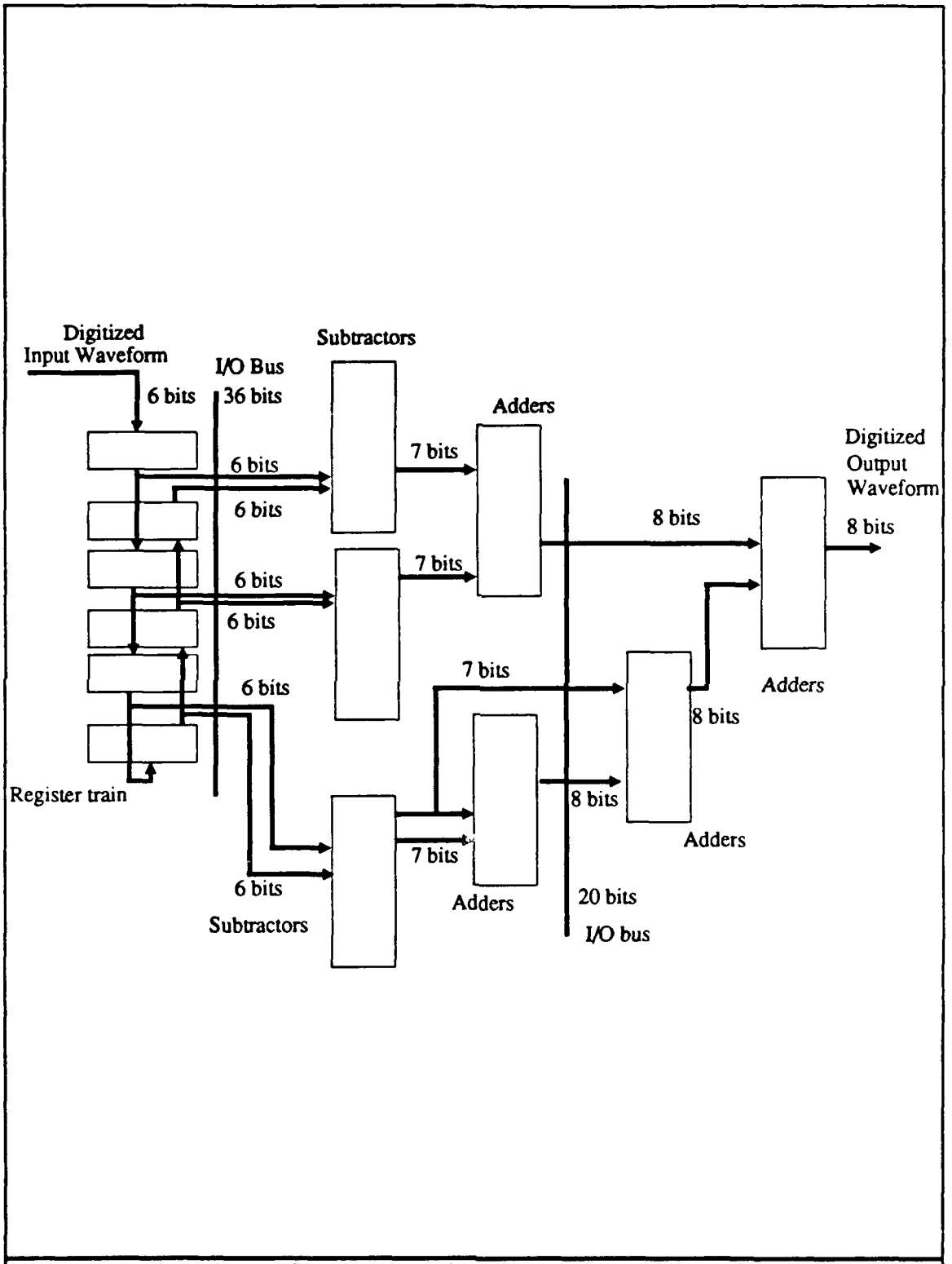


Figure 2. Hilbert transform VLSI implementation.

The circuit must store samples of the input waveform from the previous cycles in order to perform the function. These values are the first to be transferred off-chip via the bus structure. Each data bit of the past five even phases and the current signal are passed off-chip by selecting the first bus via the select1 signal. This signal activates the transmission gate (T-gate) array that is interspersed within the register train at the start of the Hilbert transform circuit. The three, twelve-bit arrays pass the thirty-six signals comprised of six words that are six bits in length to the output bus. The T-gate array does not prevent the signals from being passed onto the combinational logic that performs the next phase of the transform. The signals are now available off-chip as well as on-chip at the next stage.

The next stage is composed of combinational logic in the form of eight-bit adders and seven-bit subtractors. These blocks perform a partial product of the transform. The multiplication portion of the transform is handled by shifting the bits to the left, and thus performing an X/32 product of the term. One bit to the left multiplies by 16/32, two bits multiplies by 8/32, and so on, until 5 bits represent a multiplier of 1/32. These terms are then added and subtracted in order to accomplish the needed coefficients. The top left adder performs the addition of the 4/32 and the 1/32 terms. The bottom left adder adds the first partial sum of the 19/32 term. Since the bits can only create powers of two, the 19/32 term is formed by adding 2/32 plus 1/32 plus 16/32. The bottom right adder performs the addition of the previous partial product with the 16/32 term. This result is added to the top left adder result to give the Hilbert tranform output.

The chip also has the ability to be configured such that the signals from the register train may be supplanted by an off-chip signal passed on an input bus. By selecting this bus, the register train signals are no longer fed into the combinational logic. A T-gate array-pair switches the signal from the register train to the input bus. The input bus now controls the combinational logic and may be fed from any source.

In the current project, the signals are being fed from another Hilbert transform chip with select1 enabled. The output of this section is also equipped with a T-gate array to allow the partial product to be sampled off-chip. This product is then passed to a third phase of the transform where the final additions are carried out. At this point, the result is the Hilbert transform of the original input waveform.

The IC circuit version of the Hilbert transform is fabricated by MOSIS and it is supplied as unmounted IC die. In addition to these unmounted IC die several packaged die were fabricated in order to validate the Hilbert transform design prior to the incorporation into the WSI project. To facilitate the performance test, a Pin Grid Array (PGA) package socket was constructed so that the signals were accessible on a protoboard layout. The test package was placed in this setup and the six-bit input was fed a digitized sine wave. The clock was pulsed as the input changes from one signal to the next. The output of the register train was compared to the input of the previous clock cycles. This output was expected to exactly follow the input of previous cycles. The final output was compared to the mathematical form of the function and also to the expected values gathered by simulating the chip with the ESIM switch-level simulator. The simulator was fed the vectors that correspond to

the voltages being placed on the chip inputs, and the resulting outputs were calculated based upon a switch-level simulation. These tests and vectors are described in Appendix A.

Substrate

The IC die rests within the surface of the planarizing Si substrate wafer. The wafers chosen for this project were three inch diameter, n-type (100)-oriented wafers that were no less than 375 microns thick. Any wafers thicker were etched to match this arbitrarily established thickness (375 microns). The 375 micron thickness is the same approximate thickness as the MOSIS IC die, and it affords the best access to the wafer-to-die transition region from the back-side. A thinner wafer would provide less support and make the die protrude from the back of the planar surface and cause alignment problems with the structural backing wafer. Thicker wafers could be used, as Takahashi used 400 micron thick wafers, but they would not be significantly better as a planarizing material since the face of the wafer is the determining factor [1:59]. The specific thickness of this planarizing wafer must be known because the next step in the process requires a calculation to determine the etch time through the wafer.

In order to hold the IC die, the wafer must be processed to provide a receptacle for the die. An anisotropic etch was used to create windows through the wafer that would receive the die. Figure 3 shows the wafer and die placement, as well as the overall configuration of the finished wafer. The wafers are provided with a silicon dioxide (SiO_2) mask by placing them in a steam atmosphere at a high temperature (1050 ^{o}C). Appendix C details the oxidation procedures. The mask is grown to provide protection of the Si substrate from the

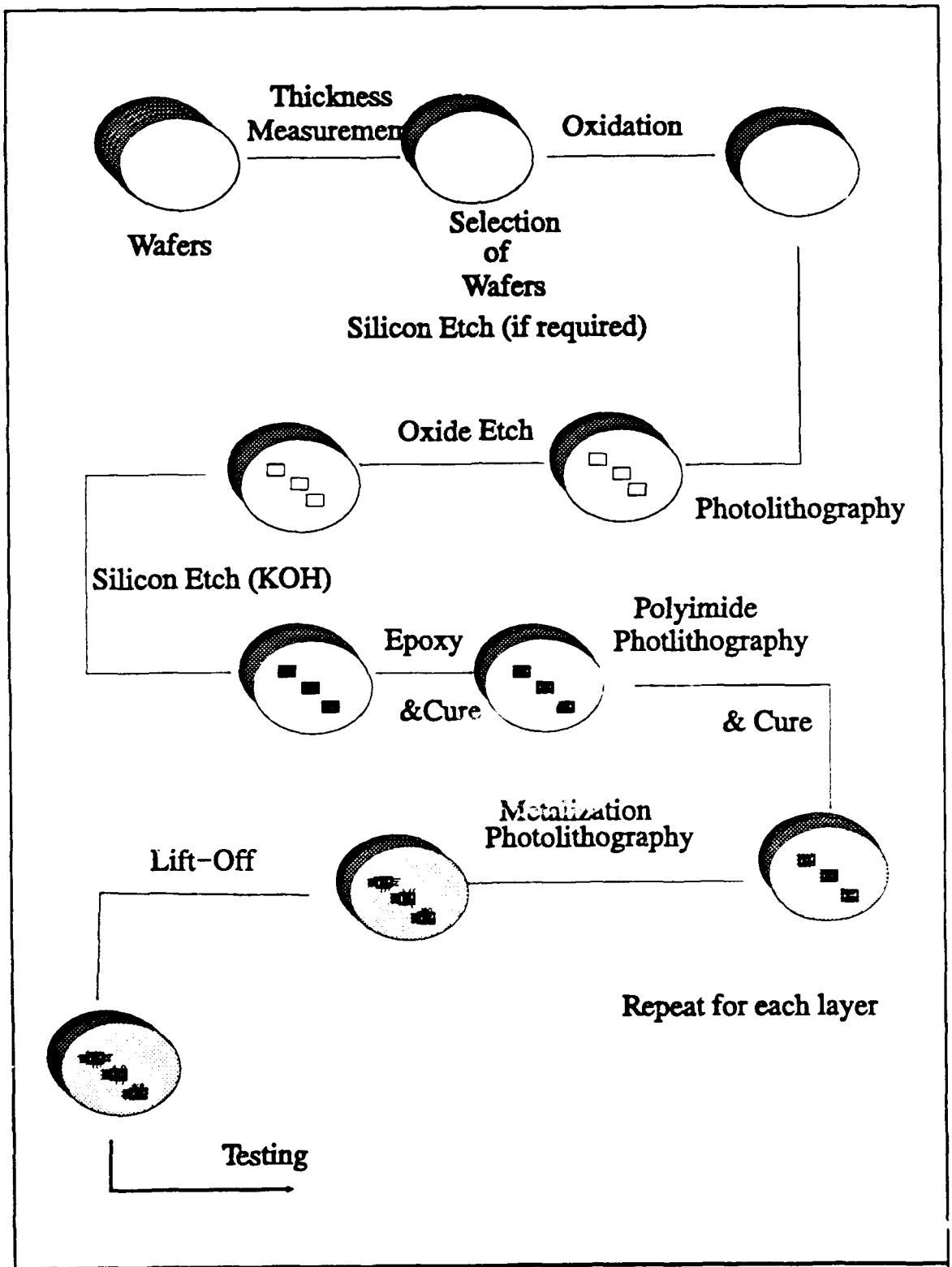


FIgure 3. WSI circuit layout.

etchant. The SiO_2 mask thickness required is established by the thickness of the wafer and the relative etch rates of the SiO_2 and the silicon. The etch rate for silicon was estimated to be 0.5 microns per minute, the oxide was estimated to be 20 Angstroms per minute. This implies that the required oxide thickness be 1.7 microns. A two micron thick SiO_2 layer was used to give a safety factor.

A potassium hydroxide (KOH) and isopropyl alcohol etchant was used to anisotropically etch the wells as described in Appendix E. The masks for the hole etch were made using the Rubylith process described in Appendix D. The SiO_2 was photolithographically processed to provide a pattern for the holes. The photoresist Shipley 111s was used as a mask for a buffered HF solution to etch the oxide to its bare silicon surface. The resist was then removed using the procedures of Appendix A, leaving the oxide mask and silicon surface to be etched. The substrate was then placed in the KOH etchant until the windows penetrated completely through the wafer, and no silicon remained in the window areas. Due to the nature of the etchant, the etch lines are formed along the planes of the silicon [10:1178-1179]. Due to this fact, the photoresist pattern must be made on the back side of the wafer since the etchant creates a 54.47^{o} angle with respect to the (100)-plane on the surface of the Si wafer. If the front side were to be used, the holes must be made wider to accommodate this slope and the transition region would be wider and would create more chances of fracturing the metal lines. The mask used is shown in Figure 4.

The Si wafers now have windows etched to hold the IC die, and the die must now be fixed into them. The epoxy used in the previous research, Master Bond EP34CA (Special)

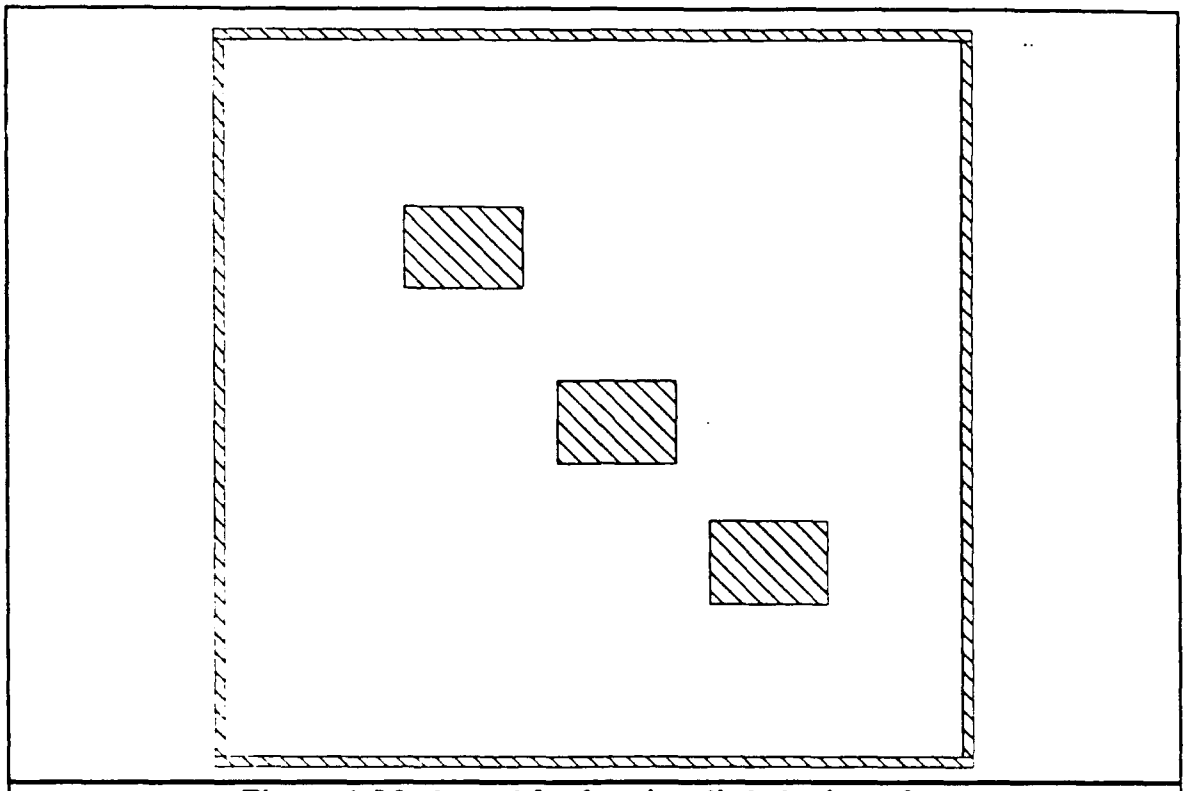


Figure 4. Mask used for forming die holes in wafer.

will again be used to hold the die in place. This material is specially formulated to match the thermal coefficient of expansion of silicon by the use of a filler of lithium aluminum silicate [11]. To implement the IC die attachment process the planarizing wafer is positioned face down onto a Teflon® block. The IC die are then placed face down into the holes, and epoxy is applied to the gap between the wafer and the die. The structure is then heated from below to 178°C in order to cure the epoxy. Weights are place on the wafer to provide good physical contact with the surface of the Teflon®. Several times during the cure, the epoxy is cleansed from the surface of the wafer in order to prevent cured epoxy from disturbing the planar surface. After one hour of cure this portion of the structure is complete. Since this structure is too thin and fragile to support itself, an unprocessed wafer is epoxied onto the

back-side of the WSI module. This forms a dual wafer structure that is approximately (375+375=) 750 microns thick.

Dielectric

Next a planarizing dielectric layer must be deposited over the WSI module's surface to facilitate the aluminum interconnection pattern. The dielectric used was Selectilux HTR 3-200 manufactured by EM Industries. This dielectric film is patternable using standard photolithographic processing procedures, and it acts as a negative photoresist material. The mask used to pattern the first level vias is show in Figure 5. The vias correspond to the bond pads on the IC die. Sloped sidewalls on these vias are important in order to prevent discontinuities in the patterned metal. The photomasks for the dielectric and subsequent layers were made from MAGIC files and plotted on film.

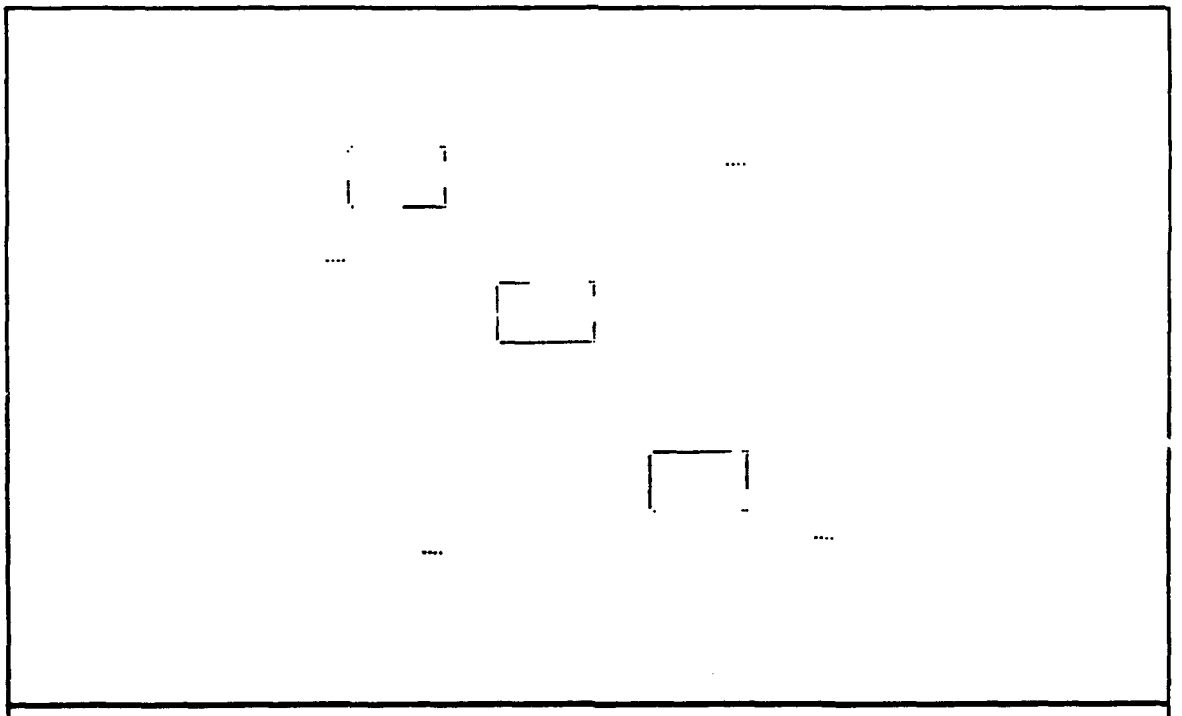


Figure 5. The first via level (die to wafer).

Photomask Process

The usual method of making photomasks for silicon wafer processing is to cut the pattern from Rubylith material and photograph the resulting image. This method was used to generate the mask for the holes described above in the Substrate section. This method is time consuming for mask layers of great complexity.

The next level photomasks contain the patterns for the vias and metal lines. These are complex images that would require many hours of cutting and peeling the Rubylith material. A new method developed in this effort had the goal of increasing the productivity of the process, and thus, make the effort more efficient. The files are created using the MAGIC CAD tool but instead of generating a Caltech Intermediate Form (CIF) file, a Calma (GDS II) file is created instead. This file can be read by the CALMA CAD station at the Electronic Technology Laboratory at Wright-Patterson AFB, Ohio, and plotted on a Versatec plotter, on film, and be used directly as a mask image. This mask image is then photographed, and the resultant plate is identical to the one that would have been created by the normal means. This process facilitates the rapid turnaround for masks that are important in the event of misalignment of the epoxied wafers.

Metalization

The metal layer is a sputtered layer of aluminum. The thickness of this layer must be approximately 1200 Angstroms, to provide satisfactory conducting paths. A two layer metal is to be used to connect the three devices used. This configuration requires two alternating

layers of the planarizing dielectric and the metal. The masks for these layers are shown in Figures 6 through 8. This completes the fabrication procedures for the wafer scale device.

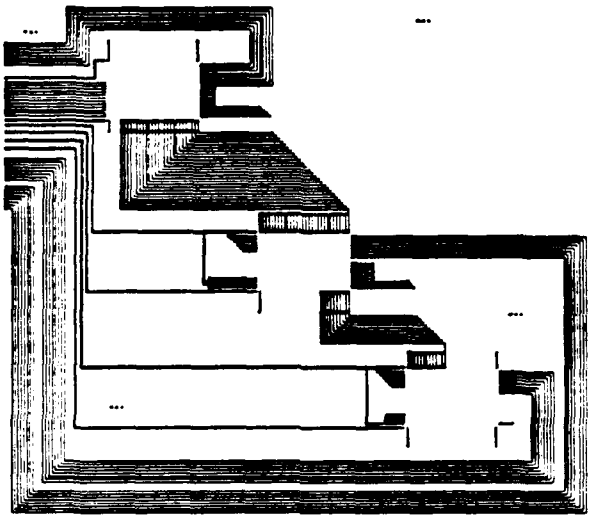


Figure 6. The first level metalization mask.

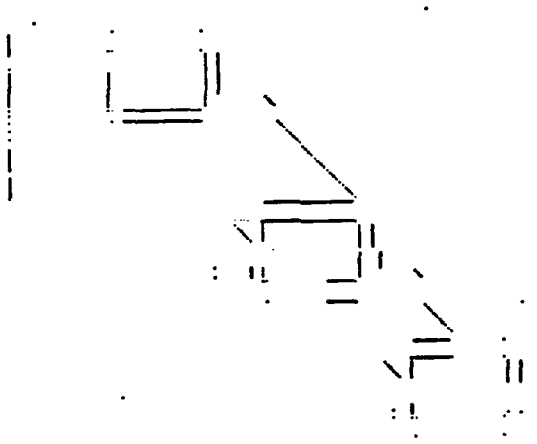


Figure 7. The interlevel via pattern.

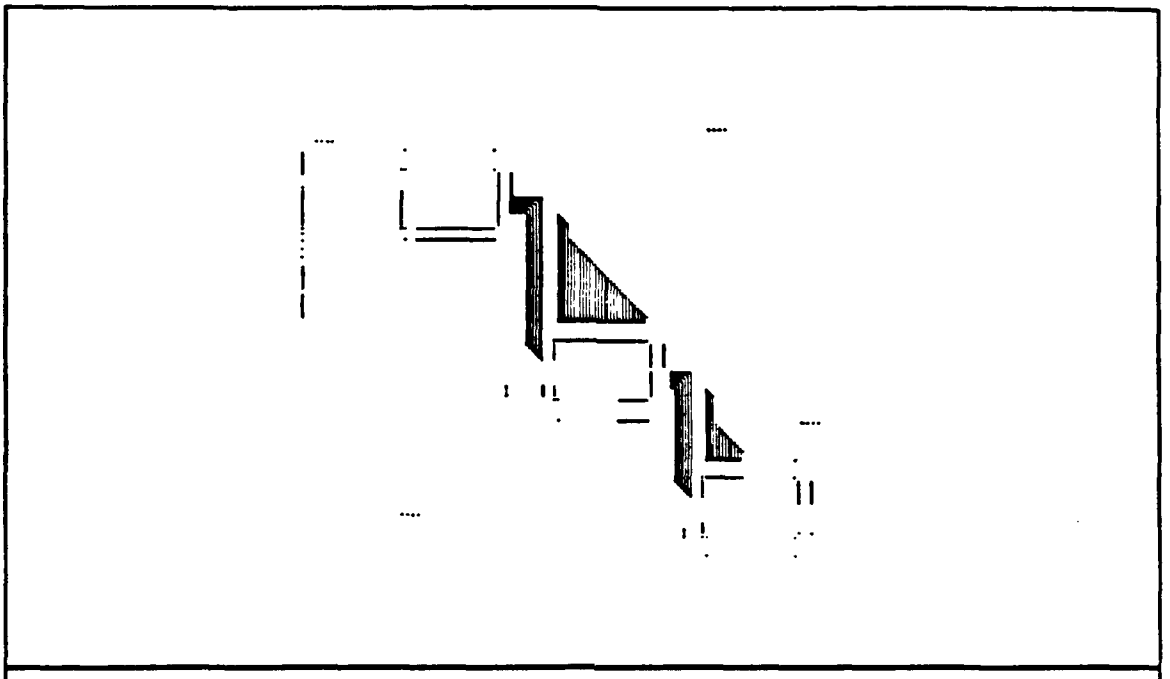


Figure 8. Second metal layer mask.

Testing

Testing of the device were accomplished by two means, mechanical step height profile evaluations of the WSI module and the electrical performance measurements of the IC die, and the metal runs. This will demonstrate the physical and electrical properties of the wafer scale integration project and show its potential and suitability for future devices.

Summary

When the procedures covered by this chapter are complete the WSI module will consist of a two wafer composite with three die mounted in a Si substrate with a two-layer metal interconnection system providing the functionality required of most current printed circuit-board level systems. Chapter IV presents the results of the fabrication processes and electrical performance tests described in this chapter.

IV. Results

The results are reported in this chapter and they are grouped into three categories: the materials, the processing, and the overall functionality of the WSI technology. The materials will be sub-divided into two sections: the materials used to implement the WSI process and those used in the tooling to fabricate the WSI product. The processing category will also be sub-divided by processing step, and the functionality topic will be discussed in a structural and electrical context. The materials will be presented first.

Materials

Teflon® Blocks

Teflon® blocks were used to support the host wafer substrate and the mounted IC die during the epoxy cure cycles. The blocks had a tendency to curl during the heating process. This was probably due to a temperature gradient across the quarter-inch thickness of the material. This curl made the resulting WSI circuit's surface non-planar. The height differential at 178°C was on the order of 3 mm from the center of the 3 inch square block to any corner. If the heat source was rapidly cycled, the height differential could be increased, but even slowly ramping the temperature to 178°C over approximately 1 hr. did not reduce the curl to an acceptable value. Without the Teflon®, the remainder of the procedures were accomplished using a glass plate. This is the same method used in previous research at AFIT [1:153-156].

The Processing

The Silicon Etch

The silicon wafer substrate etch process produced the expected results once the exposure and development times were experimentally determined. The photoresist actually used was Shipley 111s which was exposed for 2 minutes with a Karl-Suss, model MJB-UV300 mask aligner, and it was then developed until the windows retained a distilled water rinse. The development varied but was approximately three minutes by spinning the wafer at 1000 rpm using the corresponding 303A developer mixed 4:1 with distilled water. The silicon wafer was then etched for approximately fourteen hours as descibed in Appendix E. This differed by a factor of two from Takahashi's reported results but the wafers used were n-type instead of the p-type used by Takahasi. The pattern successfully etched holes completely through the silicon wafer and provided a sharp edges for the subsequent epoxy attachment of the IC die. The photograph in Figure 9 depicts one example of an etched wafer.

Epoxy

The epoxy IC attachment processing of the WSI module produced mixed results. It was difficult to work with the glass plate since most of the materials adhered to the glass as well as to the silicon. The first attempt at fabrication resulted in three die successfully epoxied into the planarizing substrate. The wafer broke while attempting to remove it from the glass, however, before the dielectric layer was applied. A structural analysis was performed to determine the suitability for the dielectric application, and it will be discussed in the functionality section.

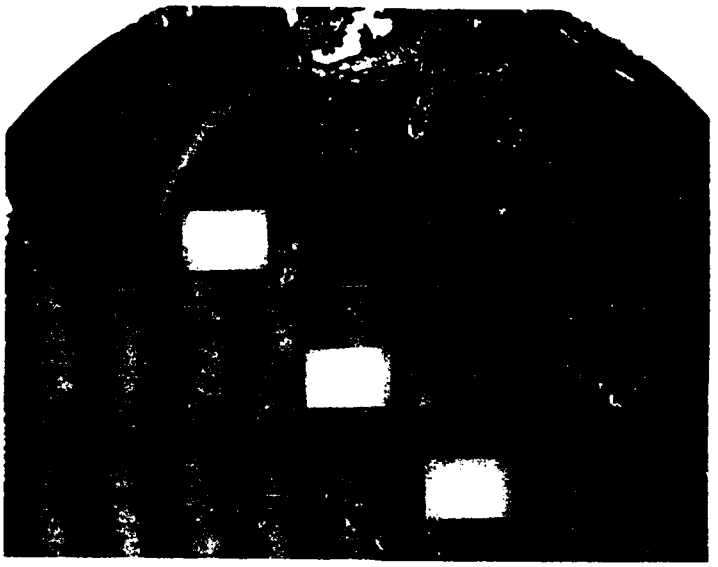


Figure 9. Wafer with etched windows for die insertion.

The next attempt used a new process that is described below in the "alternatives pursued" section. This method provided satifactory results for planarized die.

Dielectric

The dielectric was never successfully patterned onto a populated wafer module. The processing described in Appendix H was used to evaluate the dielectric on a test wafer. The wafer was printed using a large proximity separation distance as a test (the thickness of an HRP plate). This caused the vias to have sloped sidewalls, but also caused the area between the via openings to overlap. Figure 10 depicts the cross-sectional profile of a via. The dielectric was patterned using several other test wafers without successfully adhering the

dielectric to the substrate after photoprocessing. During the development of the dielectric photopattern, all of the polyimide was removed from the wafer.

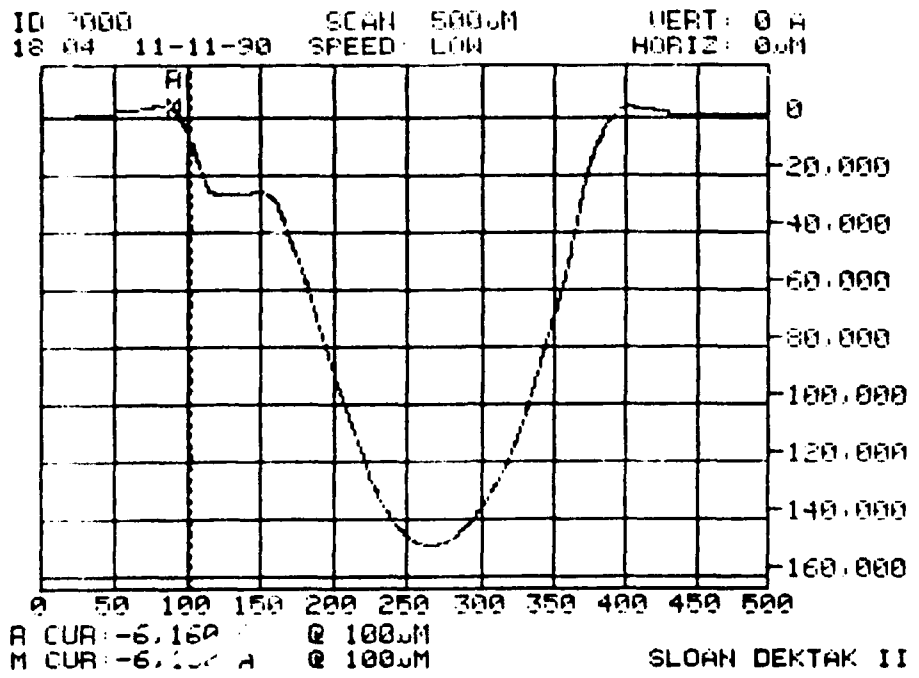


Figure 10. Cross sectional view of patterned via.

Functic nality

Structural

The first wafer with the three die epoxied into the substrate was checked for planarization using a Dektak II profilometer. The results are shown in Figure 11. In the figure, The die are the structures with the variations in surface features and the Si substrate wafer is the flat surface. None of the three die were planar or in-line with the surface of the host Si wafer substrate. One die was 7 microns high, one die was 5 microns low, and the third was tilted with a height variation of 6 to 12 microns as measured at the edge of the wafer-to-die

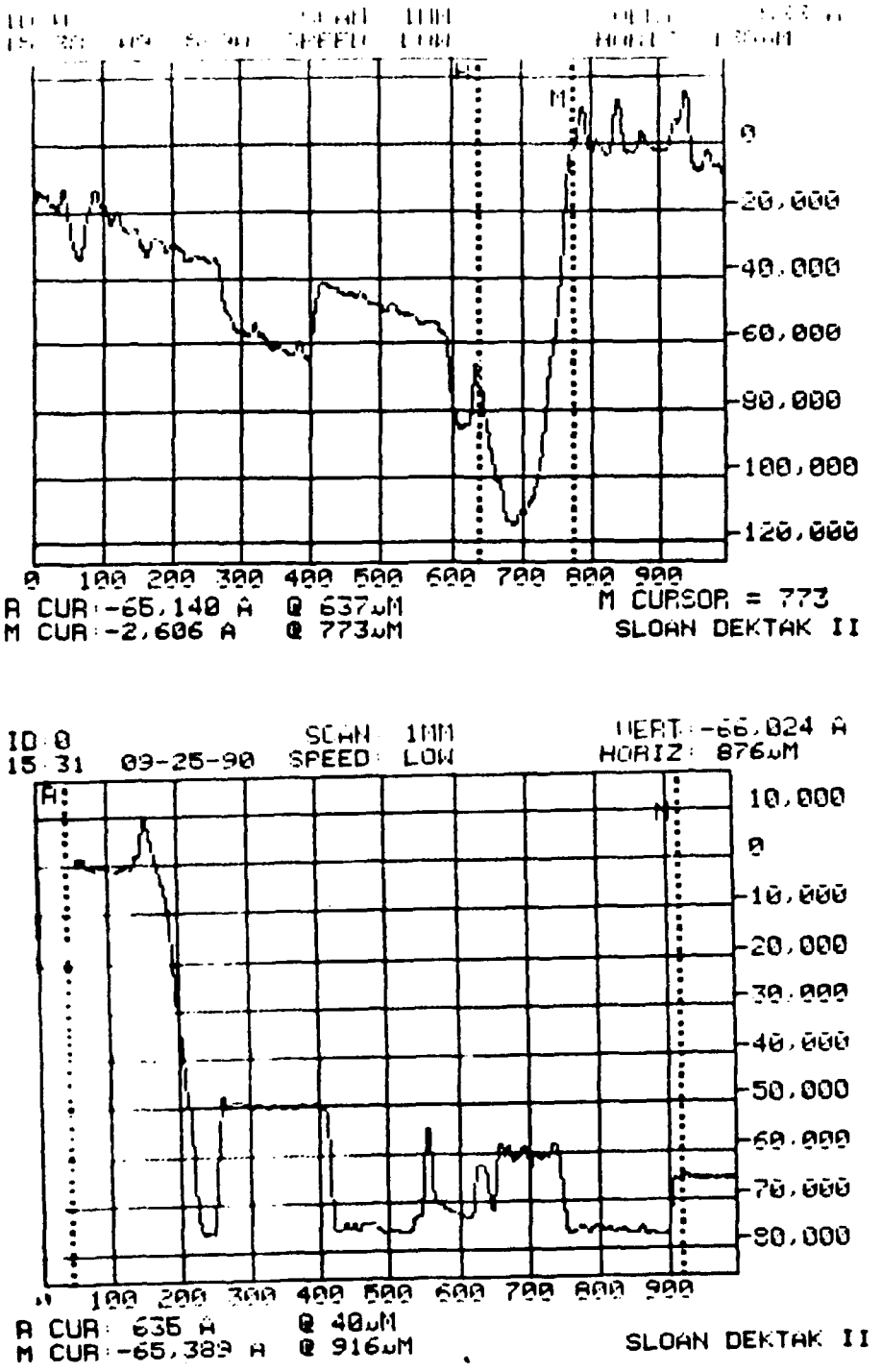


Figure 11. Profilometer Measurements of Epoxied Die.

transition. This variance was not deemed acceptable for further processing. Takahashi's results seemed to indicate that this size deviation was responsible for the break at the transition region edge [1:111].

Surface features caused by the peripheral ring material intended to align the surface of the IC die with that of the Teflon® actually caused the wafer to-die-transition region to be worse than the previously reported results. After passing over the uneven region between the wafer and die, the ring makes another transition region to the IC die surface where the bond pads are located. This characteristic can be seen in the profilometer measurements. The step height from the ring's surface to the bond pad's surface is the largest step height variance (2.5 micron), and it could possibly be limited to a short horizontal (transverse) distance (100 micron).

Electrical Tests

The electrical performance evaluation of the IC die proved to be successful. The Hilbert Transform performed its function in accordance with the data that was simulated by ESIM (Appendix A). The results shown in Figure 12 clearly establishes the operation of the transform operator in accordance with the calculated values of the equation. These correspond exactly with those predicted by the simulation.

The electrical tests of the wafer scale integrated circuit could not be performed due to the inability to realize a surface that would provide suitable vias and metal lines. If the dielectric could have been patterned on the wafer then the metal lines could have been patterned.

Alternatives Pursued

After the Teflon® block demonstrated its inability to remain flat during the epoxycure cycle, a test was run that heated the block in the oven. The block was heated at 250°C for 60 minutes an an attempt to drive off any surface impurities or reduce any internal stresses that may contribute to the curling. In addition, the block was slowly ramped up to the operating temperature to minimize the temperature gradient through the block. The block was kept at 25°C for fifteen minutes and increased by 25°C every fifteen minutes until 175°C was reached. The curl was reduced by this method but was still not planar enough to keep the die and wafer within 10 microns which was established as a design goal of this effort.

Since the Teflon® block could not be used to planarize the interface during the epoxy cure and the wafer bonded to the glass plate alignment substrate so easily if any epoxy contacted its surface, the epoxy must be kept off its surface while the wafer is face down. This requirement is detrimental to the desired processing but could not be avoided without a non-stick surface.

A method was needed that secured the IC die to the planarizing wafer. The first method attempted was to secure the IC die in the etched windows with wax. The same procedure was used as in the previous tests, but wax was used instead of epoxy. The wax is commonly used to mount a sample in the bevel-and-stain method of determining the depth of a p-n junction in a semiconductor wafer. To implement this process the wafer was heated to the wax's melting temperature, it was applied to the back side of the IC die and the host Si wafer. The wax was joined at the corners of the IC die and the etched windows to hold the die

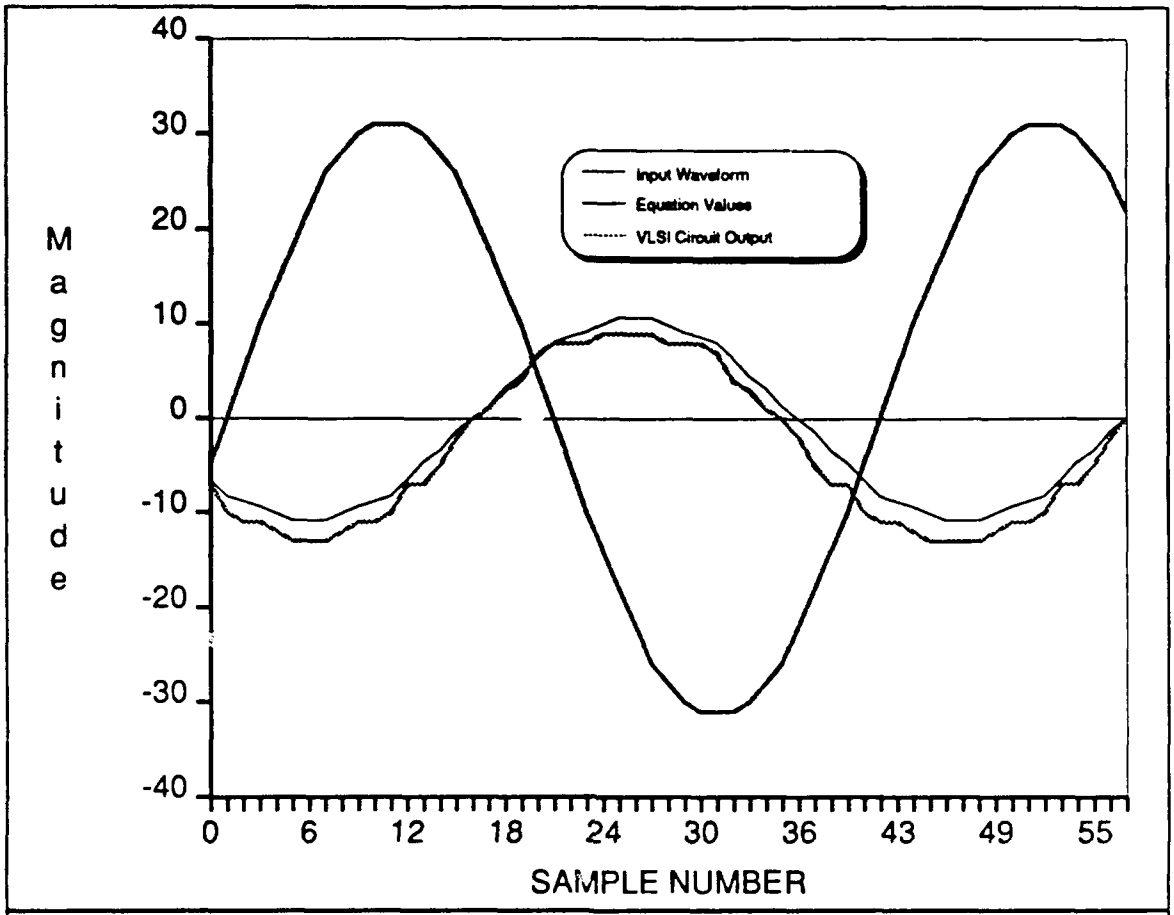


Figure 12. Hilbert Transform - Equation vs. VLSI Circui

firmly in place. It was anticipated that the the epoxy could be applied in two stages, one low temperature cure process that would fill-in large gap regions without melting the wax, and another to remelt and replace the wax. The wax did secure the die to the wafer but in the same manner as the epoxy; that is, it also secured the combination to the glass plate. Unlike the epoxy though the wax could be remelted and the die removed from the wafer and from the glass substrate.

This method was clearly as unacceptable as the previous method, due to its inability to secure the die to just the wafer in a planar fashion. However, there is one difference between the two methods. The wax method posesses the advantage of reversability.

Next, a method was devised that incorporated this desired feature without the undesirable feature of bonding to the glass substrate. Since the uncured epoxy can be disolved in acetone, the epoxy was not subjected to a high temperature cure. This allowed the epoxy to slowly gain viscosity during a 50°C processing cycle. The increased viscosity was used to hold the die and wafer together more firmly during handling. When the die and wafer are held in the planar configuration, the epoxy was applied to the back-side just as before. The heat was then increased to 50°C, and the epoxy was allowed to partially cure at this temperature. The wafer was then repositioned once the epoxy reaches a point, after 10 - 15 minutes, when the wafer can be moved without the die shifting in position. Cleaning of the surface with cotton tipped swabs, wetted with acetone, removes any surface epoxy that could cause a problem.

If at any time during this stage it is desired to remove a die, the wafer can be flooded with acetone, and the epoxy will disolve. The die may also be repositioned without being completely dislodged from the wafer. The planarity may be checked with the profilometer as described in Appendix G. The wafer-to-die transition region is now accessable to measurement, whereas in the previous method, it was always down on the surface of the glass plate. This measurement process is continued until all sides of the die are established to be planar with the surface of the wafer. This process was very successfull. Figure 13

depicts an example of the pre-cure sample profile. Once the transition region is determined to be planar, the epoxy cure may continue. The wafer is again placed in contact with the glass plate to keep the planar region from shifting and the temperature is increased to cure the epoxy.

The post cure results revealed that the IC die shifted by less than 5 microns during this epoxy cure process. The maximum deviation of the wafer to die transition was less than 10 microns and is heavily dependent on the pre-cure step height variances. The smaller the pre-cure variance, the more likely the post cure is to vary by less than five microns from the substrate surface to the surface of the IC die.

There appeared to be some areas where the void region was greater than fifteen microns. This process leads to this undesirable problem because of the need to keep the epoxy from the glass substrate. This void must be filled prior to metalization or the signal lines may not contact the IC die bond pads. Attempts to fill the void from the WSI modules front-side were not very effective, but they did provide some relief. The end result was a continuous void region that was 0 to 10 microns deep in the transition region. Near the edge of the transition region, small areas of epoxy were observed to be left on the WSI module's surface that were approximately 10 microns or less in height. Figure 14 depicts a sample of the transition region's pattern.

Alignment

Since each IC die was cut from its supporting substrate by the MOSIS fabrication foundry, there is no inherent alignment with each other except for the constraints imposed

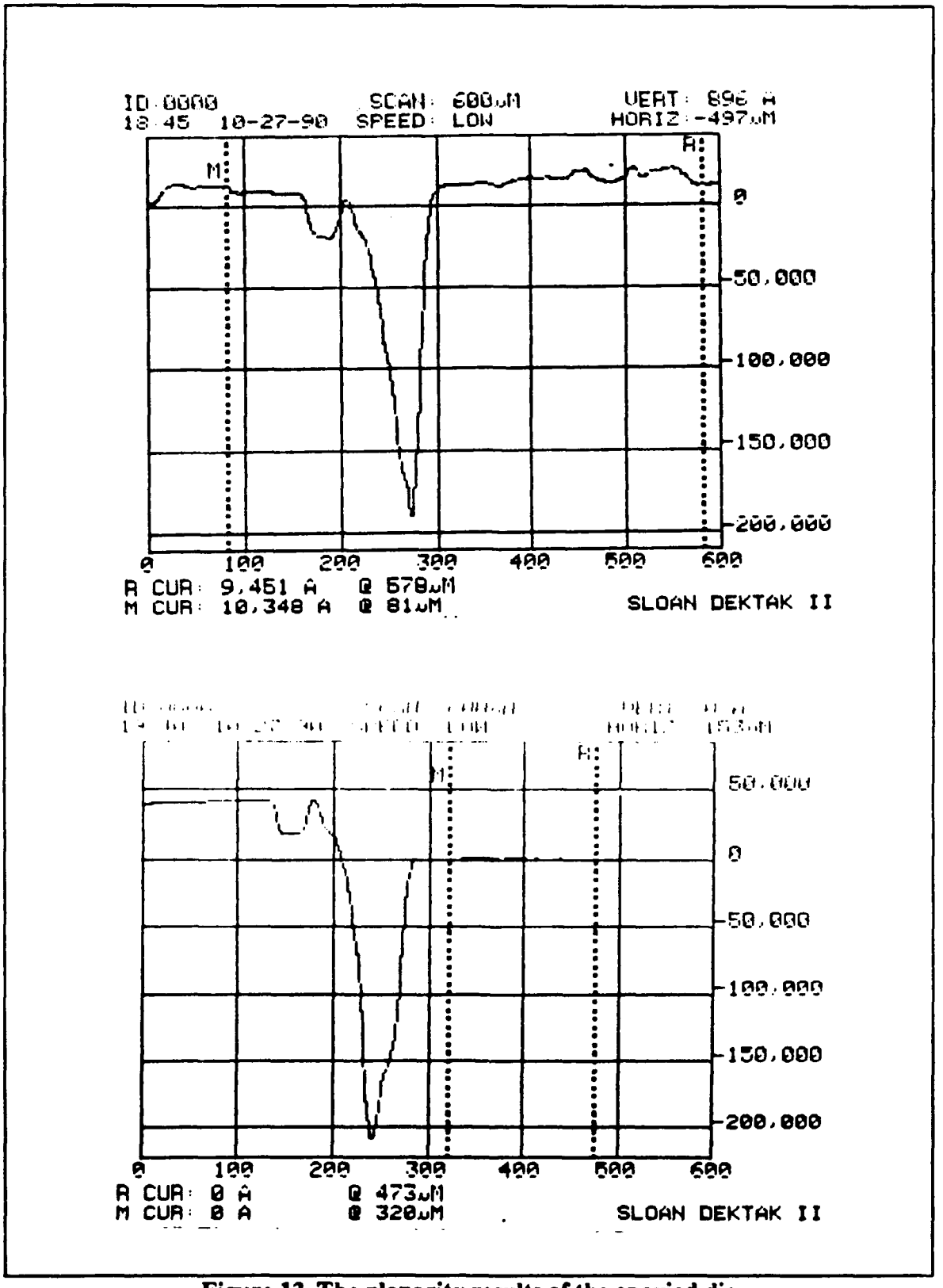


Figure 13. The planarity results of the epoxied die.

by the etched windows. In an ideal situation, the etched windows would exactly conform to the IC die size, but since the IC die have uneven edges (50 micron variation by micropsopic observation), the etched windows may be larger or smaller depending on the error in the measurement of the thickness of the wafer. The actual alignment errors are shown in Figure 14 for the sucessfully epoxied wafer. The rotational error was sufficiently close to zero for the original photomask x-y coordinate system to allow contact with the bond pads without adjustment. The errors in the x-y plane however, required that new photomasks had to be made. Appendix D describes the process of making photomasks and the alignment measurements. The new photomasks allowed all the bond sites to be contacted with the same mask.

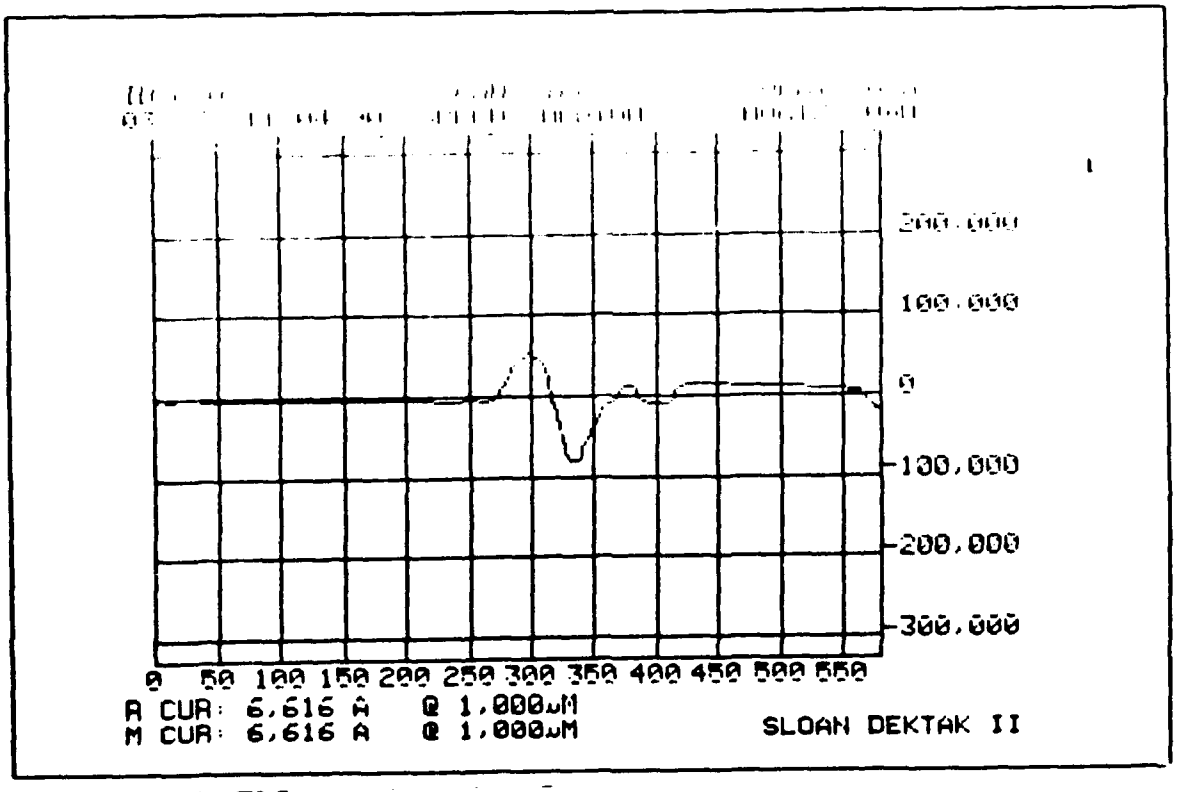


Figure 14. Edge pattern of epoxied die.

Summary

The results show a mixture of progress and problems. The Teflon® surface proved to be an excellent non-stick surface for the epoxy but the attempted method would not suffice for this research. Nonetheless, the low temperature cure process for the epoxy also provided very good results, as well as facilitating the mask alignment process. Chapter five explores the problem areas encountered and makes recomendations for future research.

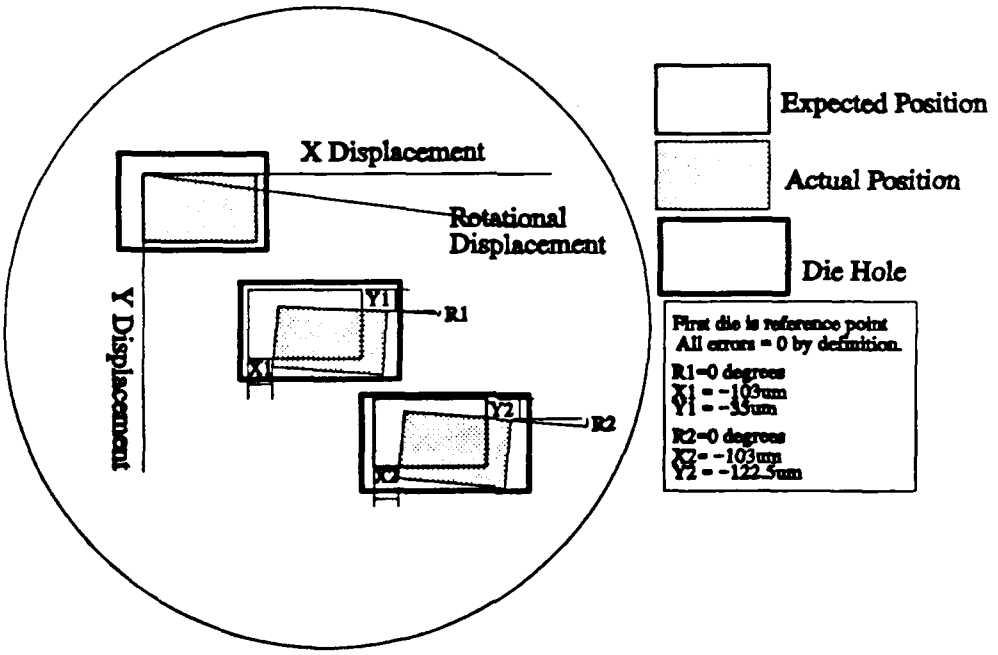


Figure 15. Displacement of die from expected position.

V. Recommendations and Conclusions

This chapter presents any recommendations for future research as they relate to the findings of the previous chapter. The recommendations will be made consistent with the deficiencies noted in the previous chapter.

Teflon®

As noted, the Teflon® alignment flat was subject to an undesirable distortion (curl) due to a thermal gradient across the material. A substitute for the block of Teflon® would be preferred that maintained the surface properties of the Teflon® and the bulk properties of the glass substrate used in this research. One potential solution to this problem would be a Teflon® coated surface as opposed to the solid block of Teflon®. If the Teflon® existed as a thin film on the surface of some more stable material; for example, a metal or ceramic, then the non-stick surface properties would be present as well as the stable planarization properties of the underlying material. The underlaying material could be machined to a smooth and flat surface, and the Teflon® thin film could be attached to the surface and then could be polished to the required degree of flatness. Berghof/America has products that could serve this purpose [13]. A spray-on Teflon® film could be used, or a thin sheet of Teflon® could be bonded to the surface with a Chemgrip™ bonding kit [13:35].

IC Design

As noted in the results, the ring of material designed to present a flat surface to the Teflon® actually disrupted the planar surface. This situation created a discontinuity on the

inner (circuit side) of the ring. As the profilometer measurements revealed, a better solution is to gradually form an interior slope. This can be accomplished by incorporating a metal1 and metal2 and polysilicon(1 and/or 2) surface, then incrementally step-down to metal1 with metal2 then down to only metal1 and finally to polysilicon only. This arangement would provide the benefits of the ring, while actually improving the gradual slope required by the vias and the wafer metal lines on the interior of the chip.

Another solution to this problem would be to design the IC chip so that the wafer bond pads are on the interior of the die. The reason most bond pads are arranged along the perimeter of most ICs is to facilitate the wire bonding process. The wire bonding process requires that the bond wires do not cross each other, additionally and MOSIS design rules limit the size and placement of the bond pads as well. These limitations do not apply to WSI and thus, a more efficient scheme for situating bond sites may be employed that incorporates this advantage of the WSI technology.

Conclusions

The major problem to be tackled by this investigation is the die-to-wafer transition region irregularity caused by the processing limitations of the WSI technology. This research has shown that a low temperature process and subsequent high temperature epoxy cure are sufficient to produce a transition region which is essentially planar. The resulting transition region deviation should be suitable for future WSI efforts and conforms to the original requirement for a simple, straightforward processing scheme to implement the WSI technology using VLSI die fabricated by conventional processing. A new method of creating

photomasks that can be quickly modified using the die placement information was also developed. This new capability will facilitate the WSI effort by allowing the photomasks for succesive layers to be created after the initial die attach process without lengthening the overall fabrication cycle. This investigation also highlighted the problems still to be solved in order to produce a completely functional WSI circuit. The first of these problems was the inability of the Teflon® to provide a planar surface. The next problem was the inability to pattern the dielectric onto a wafer-scale module. The wafer-scale technology research area requires a full scale module to be designed and fabricated in order to provide adequate electrical characterization to demonstrate the benefits of the technology.

Appendix A ESIM Test Procedures and Results

Software Packages Required:

ESIM - Event Driven Switch Level Simulator

MAGIC - VLSI Layout Editor

MEXSCP - SIM File Conversion Tool (UCB cadtools MEXTRA)

CSTAT - Circuit Status Checking Utility

Description of the Process:

The ESIM package uses a SIM file (defined by the UCB cadtools) which describes the circuit on a gate level. The circuit was first developed using the MAGIC software and converted to Caltech Intermediate Form (CIF). This file was then converted using the MEXSCP utility to the SIM form. This file was then used to perform the simulation of the circuit using ESIM. Test vectors were developed to provide required inputs to the system, and the simulator determines the operation of the system by passing the values according to a switch-level transistor model. (If the gate has the required logic signal, then the input is passed to the output). No determination of losses are provided. This exercise provides an expected value table for the actual circuit when subjected to the same test conditions, and it gives a confidence factor to the designer that the layout actually performs the intended function.

The Hilbert transform circuit was divided into three logical sections. Each section was tested using a digitized sine wave input to the Hilbert transform circuit. The resultant signals were sampled at each of the two internal section boundaries as well as at the external Hilbert transform's output. The middle section was also tested by inputing the same values of the

register train output into the subtractor inputs by using the first input bus selector. The results of this test were compared to the signals obtained when the Hilbert transform was allowed to drive the output buses. The same type of test was performed on the final adders using the second input bus.The output buses are non-destructive, so the final transform output is read in each case to verify proper circuit operation.

The Process:

Step 1. Create the circuit layout with the MAGIC tool.

Step 2. Generate a CIF file using the command ":cif write" or ":cif" from within MAGIC.

Step 3. Convert the CIF file to a SIM file using the MEXSCP utility. (On AFIT systems this conversion utility is available on ORION.AFIT.AF.MIL)

Step 4. The CSTAT software package may be used to verify that the signals propagate through the circuit, and that outputs can be changed. This is useful to eliminate short circuits to Vdd or GND and unconnected I/O Pads.

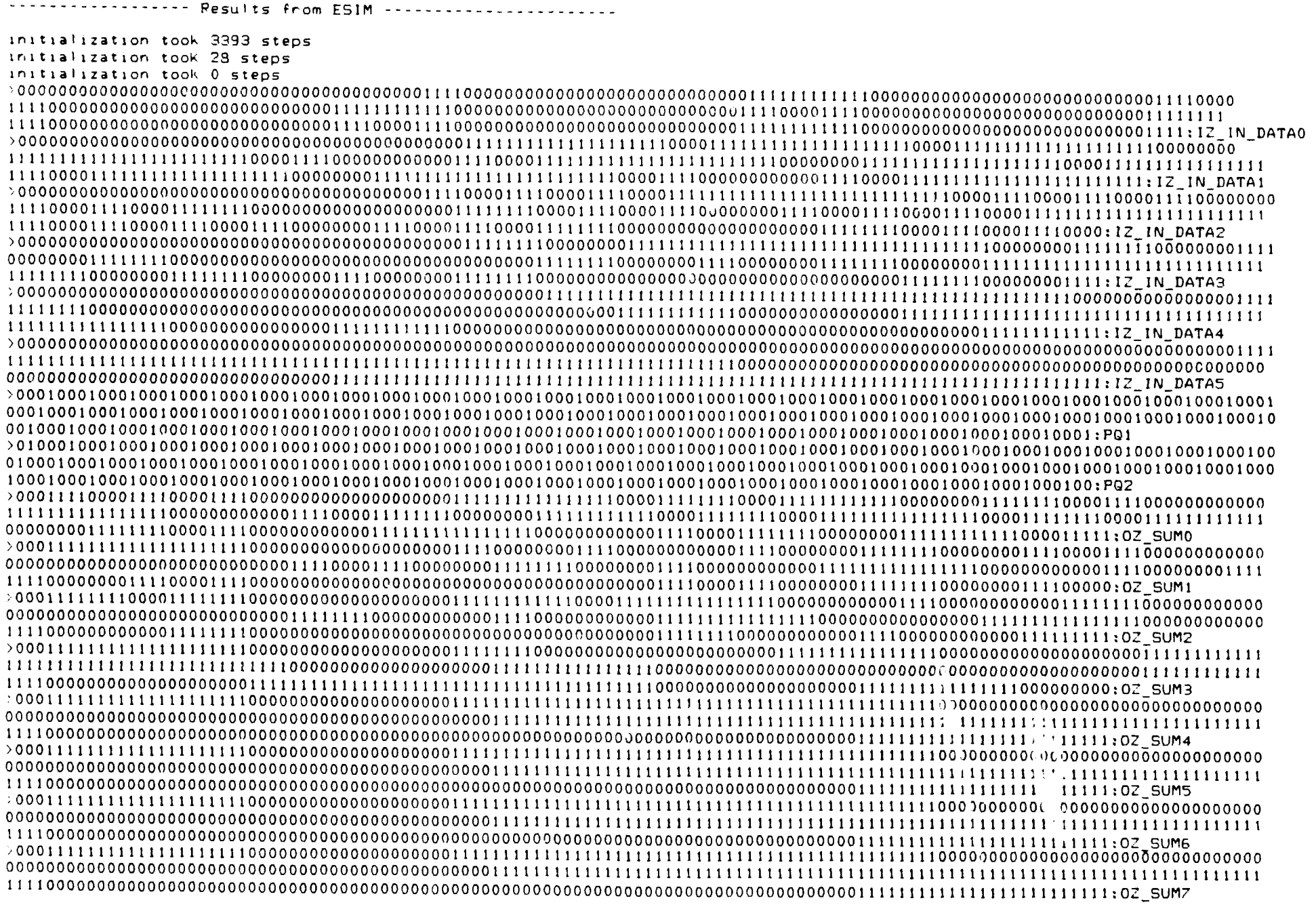
Step 5. Create ESIM test vector files (using any text editor) that contain the ESIM input vectors and signals that are to be output. This data must be in the prescribed command file structure. (l signalname ; h signalname ; v signalname ; w signalname ... etc.).

Step 6. Run ESIM using the following syntax: "esim input_simfile.sim -outputfile". When ESIM returns enter the name of any test vector files required: @testfile1. This exercise will create a file called "outputfile" that contains the results of any watched vectors from the circuit.

Step 7. Send the circuit to the MOSIS foundry for fabrication when the test results indicate proper operation is performed by the layout. (Other tools may be used to verify operation prior to fabrication; for example SPICE, but it was not used in this investigation.)

The following pages contain the test vector files and the results obtained from the ESIM program.

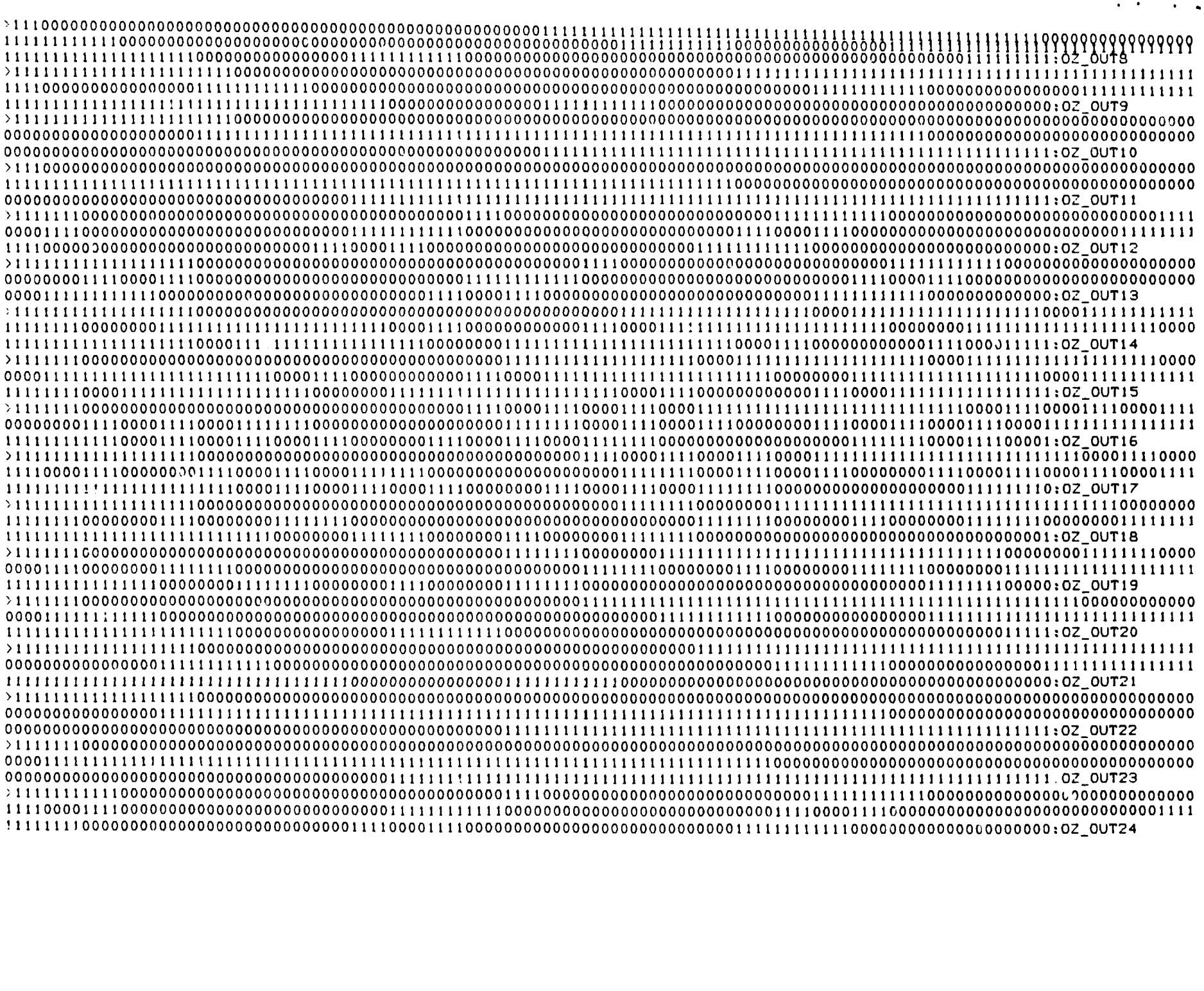
```
h Vdd
l GND
l IZ_BUS_Select_1
l IZ_BUS_Select_2
l IZ_BUS_Select_3
l IZ_BUS_Select_4
I
I
I
V IZ_IN_DATA0  0000000000000000000000000000000000000001110000000000000000000000000000001111111111100000000000000000000000000
0000111100001111000000000000000000000000000011111111111000000000000000000000000000011110000111100000000000000000000000000
1111111111110000000000000000000000000000011110000111100000000000000000000000000011111111111100000000000000000000000001111
V IZ_IN_DATA1  0000000000000000000000000000000000000000011111111111111111111000011111111111111111111000011111111111111111
1111000000001111111111111111111111111111000011110000000000000111100001111111111111111111111111100000000111111111111111111111100001111
1111111111111111000011111111111111111111100000000111111111111111111111111110000111100000000000001111000011111111111111111111111111
V IZ_IN_DATA2  0000000000000000000000000000000000000000111100001111000011110000111111111111111111111111111111000011110000111
0000111100000000111100001111000011111111000000000000000000000011111111000011110000111100000000111100001111000011110000111111
1111111111111111111100001111000011110000111100000000111100001111000011111111000000000000000000000000111111110000111100001111000
V IZ_IN_DATA3  0000000000000000000000000000000000000000001111111100000000111111111111111111111111111111111111111000000001111
1111000000000111100000000111111110000000000000000000000000000000000000000111111110000000011110000000011111111000000000111111111111
1111111111111111111111111000000000111111110000000001111000000000111111110000000000000000000000000000000000000000111111110000000001111
V IZ_IN_DATA4  0000000000000000000000000000000000000000000011111111111111111111111111111111111111111111111111111111111110000
0000000000001111111111110000000000000000000000000000000000000000000000000111111111111000000000000000011111111111111111111
1111111111111111111111111111110000000000000000011111111111100000000000000000000000000000000000000000000000000011111111111
V IZ_IN_DATA5  00000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000
0000000000011111111111111111111111111111111111111111111111111111111111111111111111111000000000000000000000000000000000000000
0000000000000000000000000000000000000000000000111111111111111111111111111111111111111111111111111111111111111111111111111111
V PQ2          0100010001000100010001000100010001000100010001000100010001000100010001000100010001000100010001000100010001000
1000100010001000100010001000100010001000100010001000100010001000100010001000100010001000100010001000100010001000100010001000
1000100010001000100010001000100010001000100010001000100010001000100010001000100010001000100010001000100010001000100010000100
V PQ1          0001000100010001000100010001000100010001000100010001000100010001000100010001000100010001000100010001000100010000100
0100010001000100010001000100010001000100010001000100010001000100010001000100010001000100010001000100010001000100010001000
1000100010001000100010001000100010001000100010001000100010001000100010001000100010001000100010001000100010001000100010001
w IZ_IN_DATA0 IZ_IN_DATA1 IZ_IN_DATA2 IZ_IN_DATA3 IZ_IN_DATA4 IZ_IN_DATA5
w PQ1
w PQ2
w OZ_SUM0 OZ_SUM1 OZ_SUM2 OZ_SUM3 OZ_SUM4 OZ_SUM5 OZ_SUM6 OZ_SUM7
c
q
```

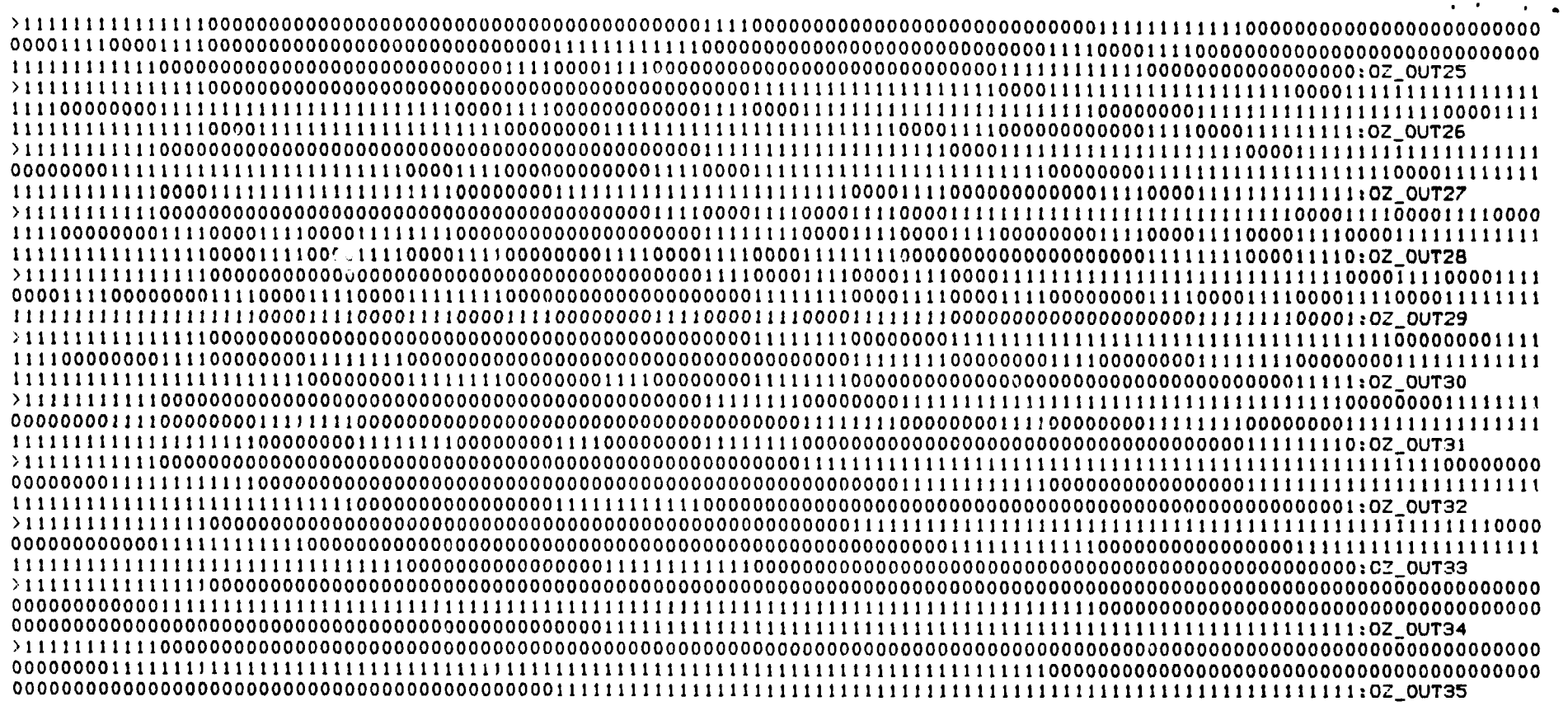

---------- Results from ESIM ----------
initialization took 3393 steps
initialization took 28 steps
initialization took 0 steps
:IZ_IN_DATA0
:IZ_IN_DATA1
:IZ_IN_DATA2
:IZ_IN_DATA3
:IZ_IN_DATA4
:IZ_IN_DATA5
:PQ1
:PQ2
:OZ_SUM0
:OZ_SUM1
:OZ_SUM2
:OZ_SUM3
:OZ_SUM4
:OZ_SUM5
:OZ_SUM6
:OZ_SUM7

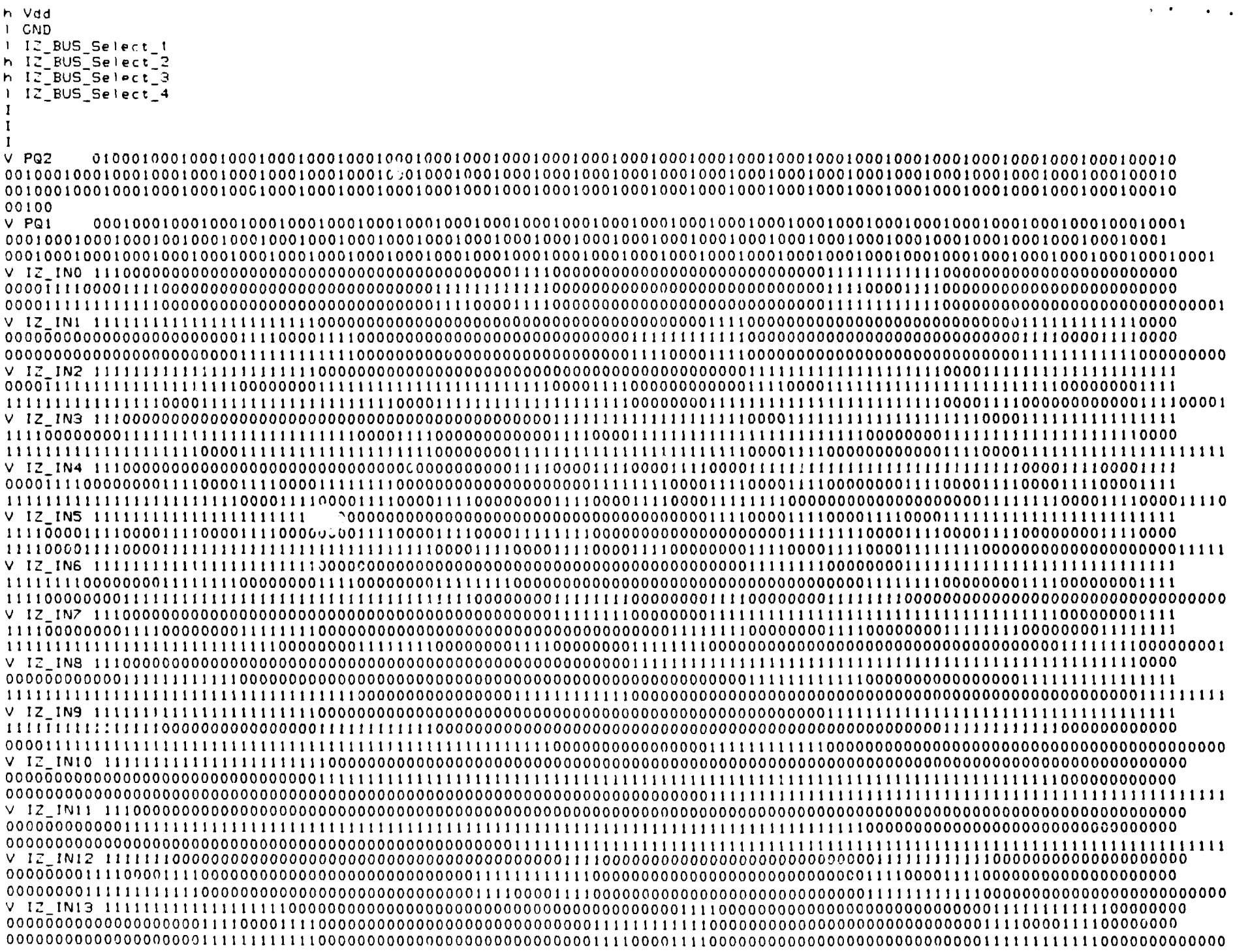
```
h Vdd
l GND
h IZ_BUS_Select_1
l IZ_BUS_Select_2
l IZ_BUS_Select_3
l IZ_BUS_Select_4
I
I
I
V IZ_IN_DATA0  0000000000000000000000000000000000000000011110000000000000000000000000011111111111000000000000000000000000000
1111000011110000000000000000000000000000111111111111000000000000000000000000000011110000111100000000000000000000000000011111111
1110000000000000000000000000000011110000111100000000000000000000000000000011111111111100000000000000000000000000001111
V IZ_IN_DATA1  0000000000000000000000000000000000000000000001111111111111111111110000111111111111111111111100001111111111111111111
0000000011111111111111111111111111000011110000000000001111000011111111111111111111111100000000111111111111111111110000111111111111
1111111000011111111111111111111111000000001111111111111111111111111000011110000000000011110000111111111111111111111111
V IZ_IN_DATA2  0000000000000000000000000000000000000000011110000111100001111000011111111111111111111111111111110000111100001111000011
1110000000011110000111100001111111100000000000000000001111111100111100001111000000001111000011110000111100001111111111111111
1111111110000111100001111000011110000000011110000111100001111111100000000000000000001111111100001111000011110000
V IZ_IN_DATA3  0000000000000000000000000000000000000000011111111000000001111111111111111111111111111111111111110000000011111111
0000000011110000000011111111100000000000000000000000000000000000000001111111100000000111100000000111111110000000011111111111111111
1111111111111110000000011111111100000000111000000001111111100000000000000000000000000000000000000011111111000000001111
V IZ_IN_DATA4  0000000000000000000000000000000000000000000000000000000011111111111111111111111111111111111111111111111111111100000000
0000000011111111111110000000000000000000000000000000000000000000000000000000000111111111110000000000000001111111111111111111111111
1111111111111111111111000000000000000011111111111100000000000000000000000000000000000000000000000000000011111111111
V IZ_IN_DATA5  0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000
0000000011111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111100000000000000000000000000000000000000000000000000
0000000000000000000000000000000000000000111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111111
V PQ2          0100010001000100010001000100010001000100010001000100010001000100010001000100010001000100010001000100010001000100010001000100
0100010001000100010001000100010001000100010001000100010001000100010001000100010001000100010001000100010001000100010001000100010001000
1000100010001000100010001000100010001000100010001000100010001000100010001000100010001000100010001000100010001000100010001000100010001
V PQ1          0001000100010001000100010001000100010001000100010001000100010001000100010001000100010001000100010001000100010001000100010001
0001000100010001000100010001000100010001000100010001000100010001000100010001000100010001000100010001000100010001000100010001000100010
0010001000100010001000100010001000100010001000100010001000100010001000100010001000100010001000100010001000100010001000100010001
w IZ_IN_DATA0 IZ_IN_DATA1 IZ_IN_DATA2 IZ_IN_DATA3 IZ_IN_DATA4 IZ_IN_DATA5
w PQ1
w PQ2
w OZ_OUT0 OZ_OUT1 OZ_OUT2 OZ_OUT3 OZ_OUT4 OZ_OUT5 OZ_OUT6 OZ_OUT7
w OZ_OUT8 OZ_OUT9 OZ_OUT10 OZ_OUT11 OZ_OUT12 OZ_OUT13 OZ_OUT14 OZ_OUT15
w OZ_OUT16 OZ_OUT17 OZ_OUT18 OZ_OUT19 OZ_OUT20 OZ_OUT21 OZ_OUT22 OZ_OUT23
w OZ_OUT24 OZ_OUT25 OZ_OUT26 OZ_OUT27 OZ_OUT28 OZ_OUT29 OZ_OUT30 OZ_OUT31
w OZ_OUT32 OZ_OUT33 OZ_OUT34 OZ_OUT35
G
q
```

------- the resultant output from ESIM ----------------

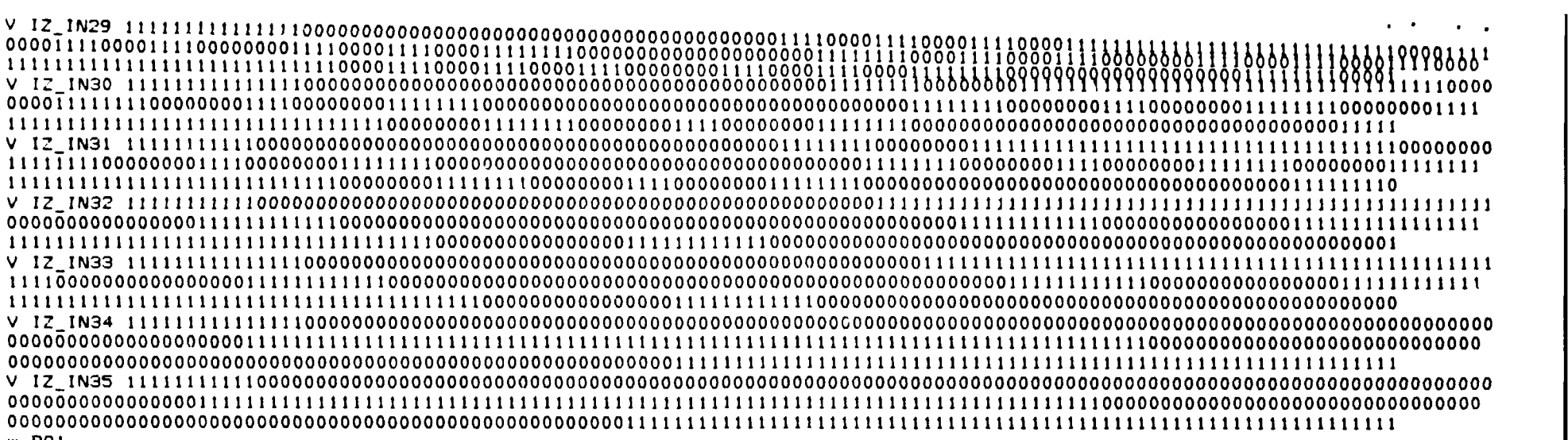
```
initialization took 3393 steps
initialization took 28 steps
initialization took 0 steps
```


OZ_OUT8
OZ_OUT9
OZ_OUT10
OZ_OUT11
OZ_OUT12
OZ_OUT13
OZ_OUT14
OZ_OUT15
OZ_OUT16
OZ_OUT17
OZ_OUT18
OZ_OUT19
OZ_OUT20
OZ_OUT21
OZ_OUT22
OZ_OUT23
OZ_OUT24

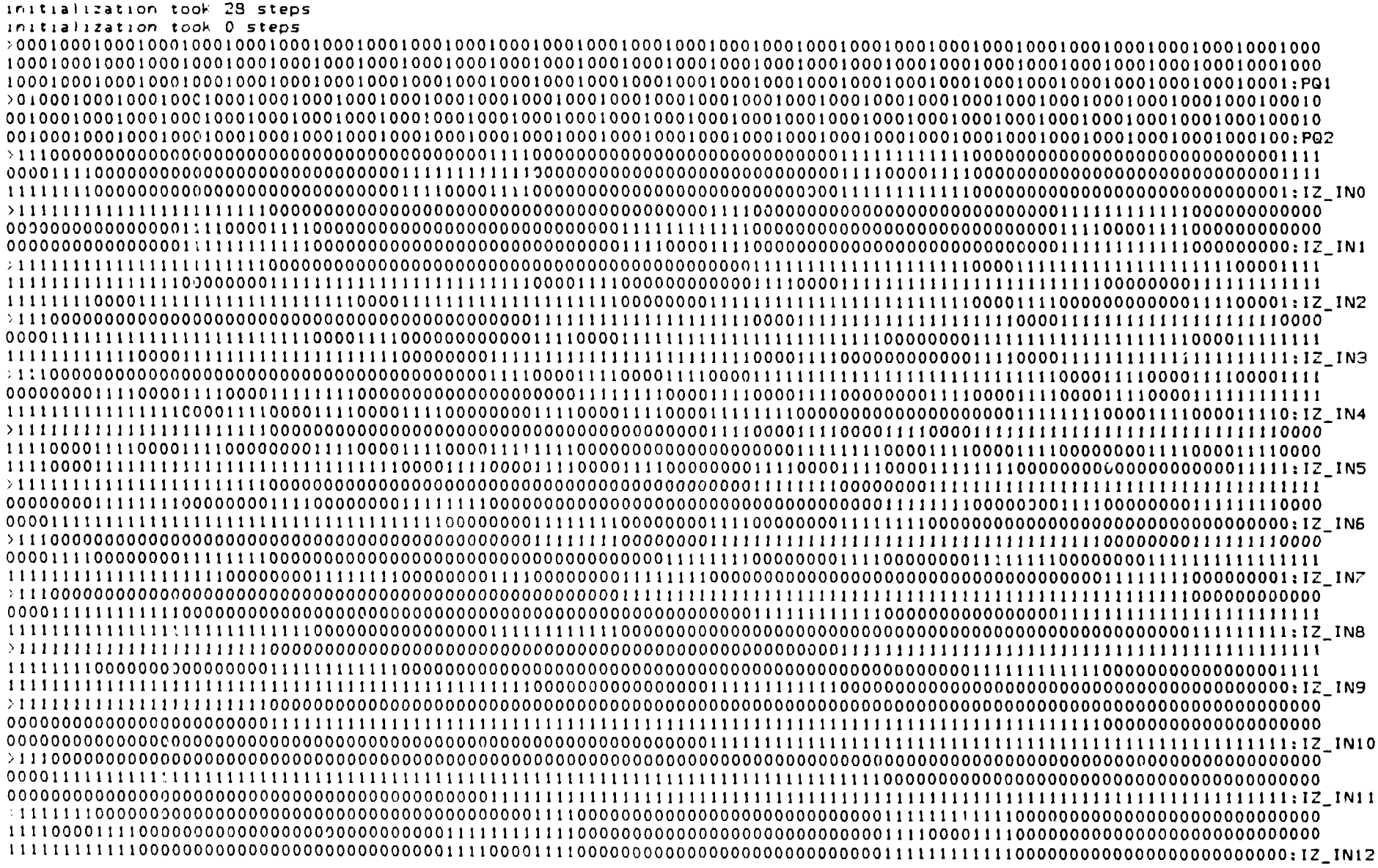

OZ_OUT25
OZ_OUT26
OZ_OUT27
OZ_OUT28
OZ_OUT29
OZ_OUT30
OZ_OUT31
OZ_OUT32
OZ_OUT33
OZ_OUT34
OZ_OUT35

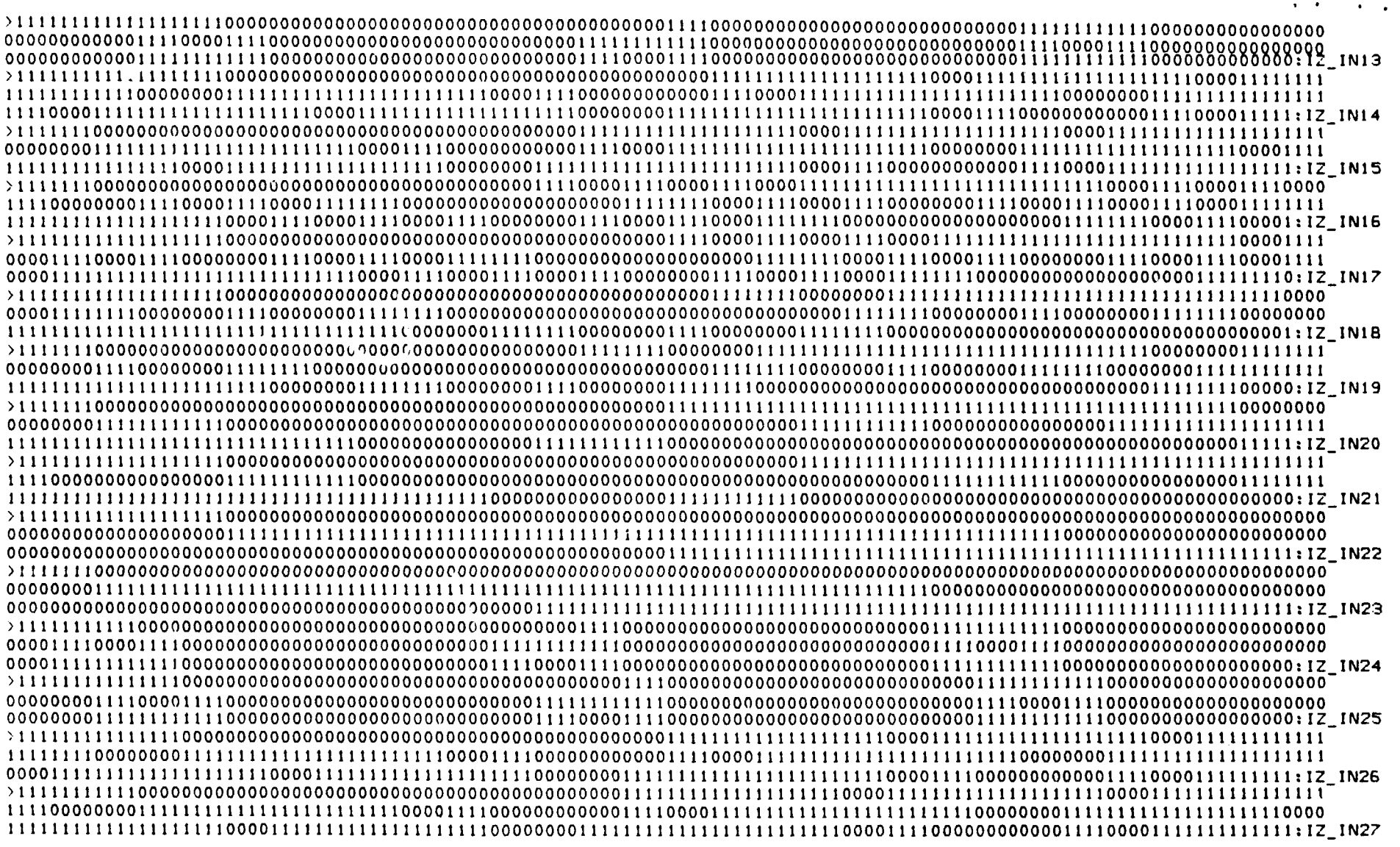

h Vdd
l GND
l IZ_BUS_Select_1
h IZ_BUS_Select_2
h IZ_BUS_Select_3
l IZ_BUS_Select_4
V PQ2
V PQ1
V IZ_IN0
V IZ_IN1
V IZ_IN2
V IZ_IN3
V IZ_IN4
V IZ_IN5
V IZ_IN6
V IZ_IN7
V IZ_IN8
V IZ_IN9
V IZ_IN10
V IZ_IN11
V IZ_IN12
V IZ_IN13

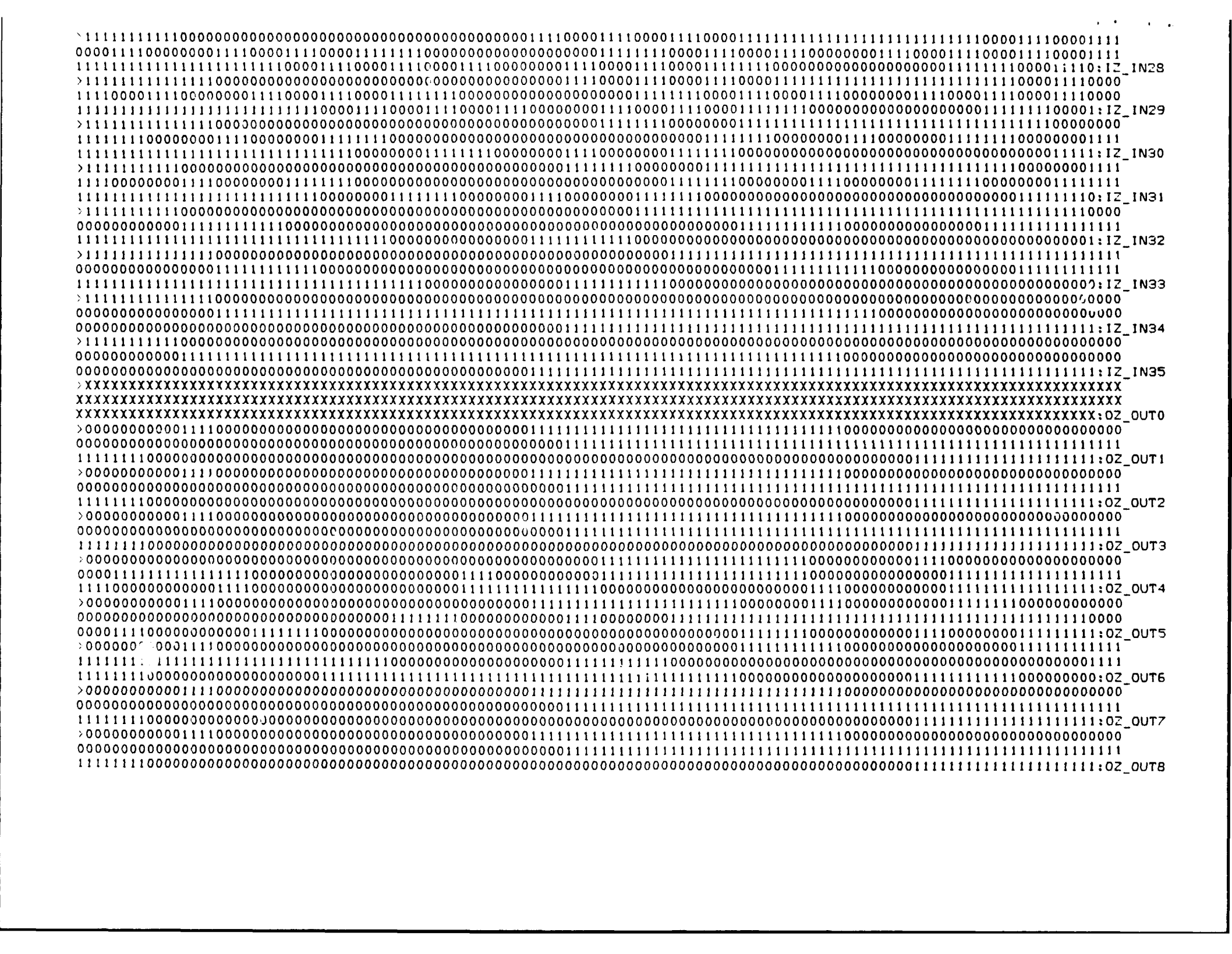

V IZ_IN14
V IZ_IN15
V IZ_IN16
V IZ_IN17
V IZ_IN18
V IZ_IN19
V IZ_IN20
V IZ_IN21
V IZ_IN22
V IZ_IN23
V IZ_IN24
V IZ_IN25
V IZ_IN26
V IZ_IN27
V IZ_IN28

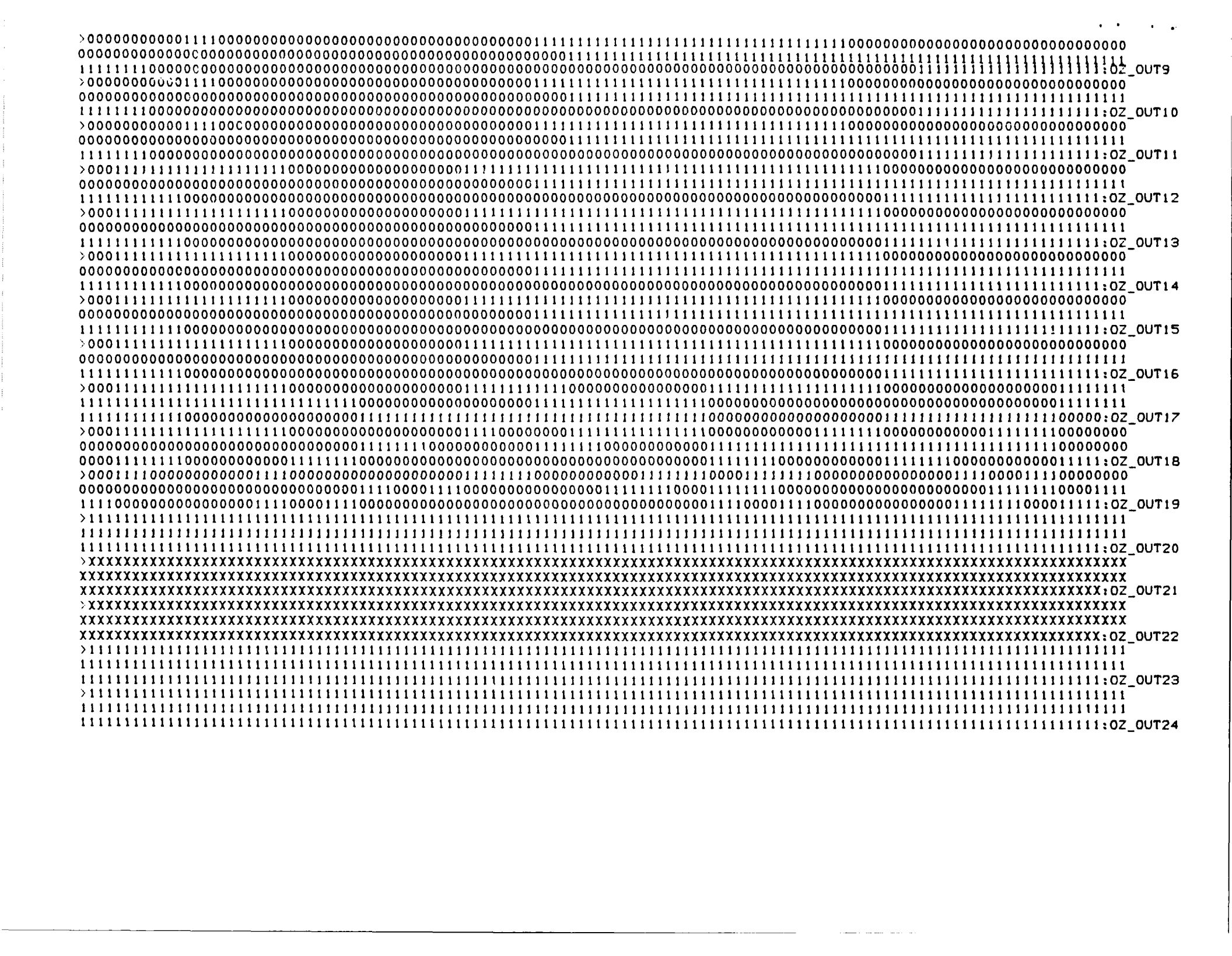


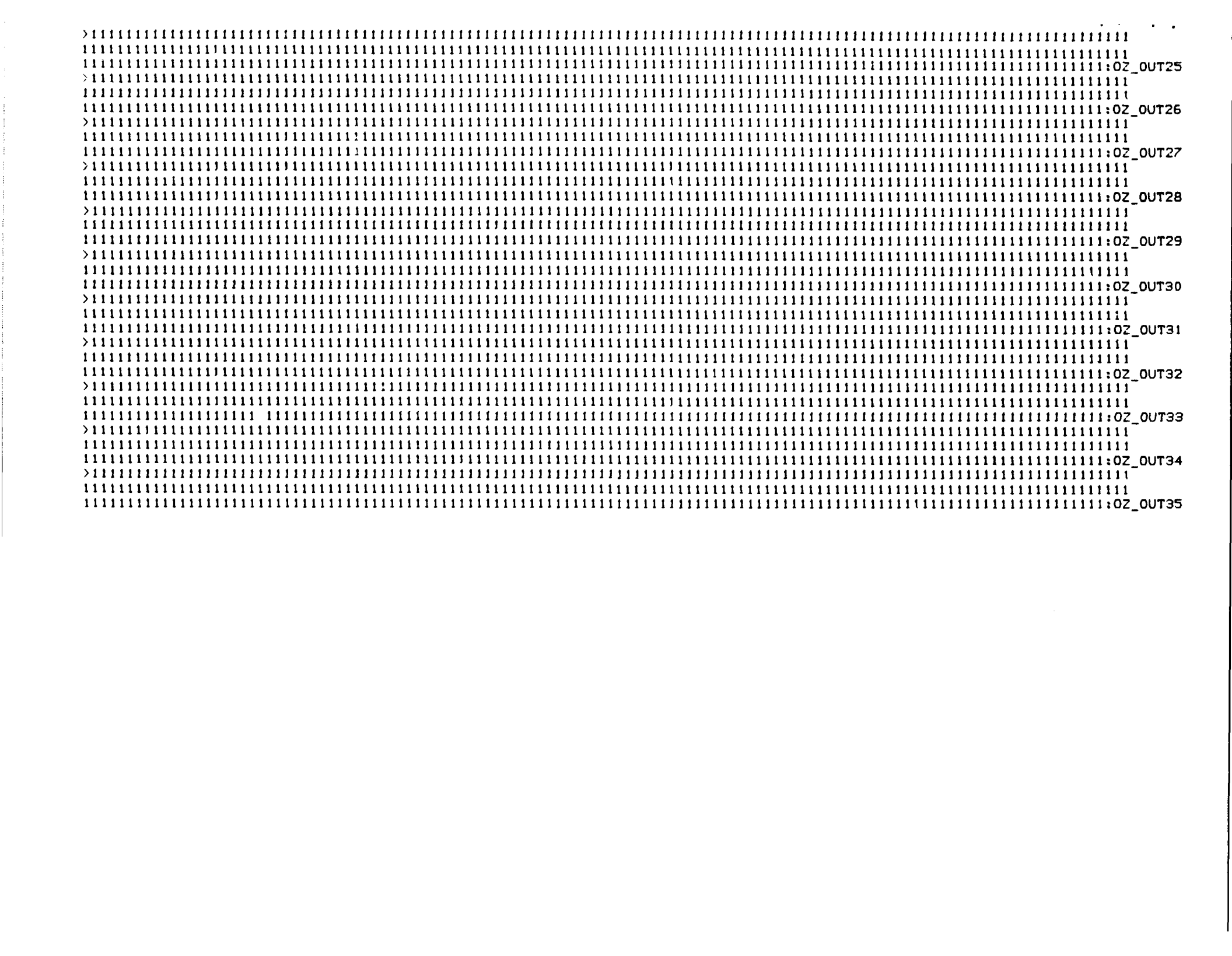

```
w PQ1
w PQ2
w IZ_IN0 IZ_IN1 IZ_IN2 IZ_IN3 IZ_IN4 IZ_IN5 IZ_IN6 IZ_IN7
w IZ_IN8 IZ_IN9 IZ_IN10 IZ_IN11 IZ_IN12 IZ_IN13 IZ_IN14 IZ_IN15
w IZ_IN16 IZ_IN17 IZ_IN18 IZ_IN19 IZ_IN20 IZ_IN21 IZ_IN22 IZ_IN23
w IZ_IN24 IZ_IN25 IZ_IN26 IZ_IN27 IZ_IN28 IZ_IN29 IZ_IN30 IZ_IN31
w IZ_IN32 IZ_IN33 IZ_IN34 IZ_IN35
w OZ_OUT0 OZ_OUT1 OZ_OUT2 OZ_OUT3 OZ_OUT4 OZ_OUT5 OZ_OUT6 OZ_OUT7
w OZ_OUT8 OZ_OUT9 OZ_OUT10 OZ_OUT11 OZ_OUT12 OZ_OUT13 OZ_OUT14 OZ_OUT15
w OZ_OUT16 OZ_OUT17 OZ_OUT18 OZ_OUT19 OZ_OUT20 OZ_OUT21 OZ_OUT22 OZ_OUT23
w OZ_OUT24 OZ_OUT25 OZ_OUT26 OZ_OUT27 OZ_OUT28 OZ_OUT29 OZ_OUT30 OZ_OUT31
w OZ_OUT32 OZ_OUT33 OZ_OUT34 OZ_OUT35
C
q
```

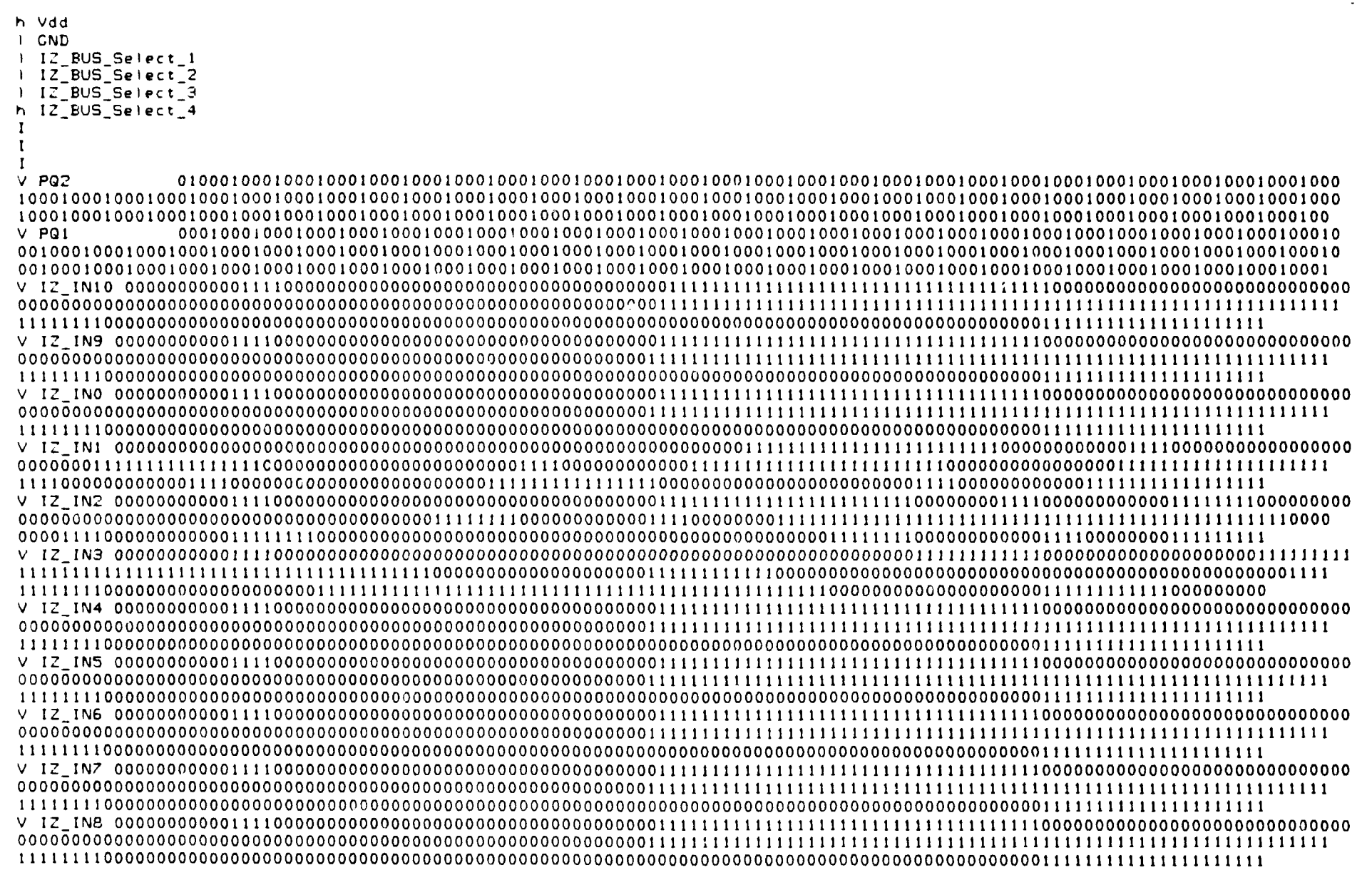

---------- ESIM OUTPUT ----------
initialization took 3393 steps
initialization took 28 steps
initialization took 0 steps
:PQ1
:PQ2
:IZ_IN0
:IZ_IN1
:IZ_IN2
:IZ_IN3
:IZ_IN4
:IZ_IN5
:IZ_IN6
:IZ_IN7
:IZ_IN8
:IZ_IN9
:IZ_IN10
:IZ_IN11
:IZ_IN12

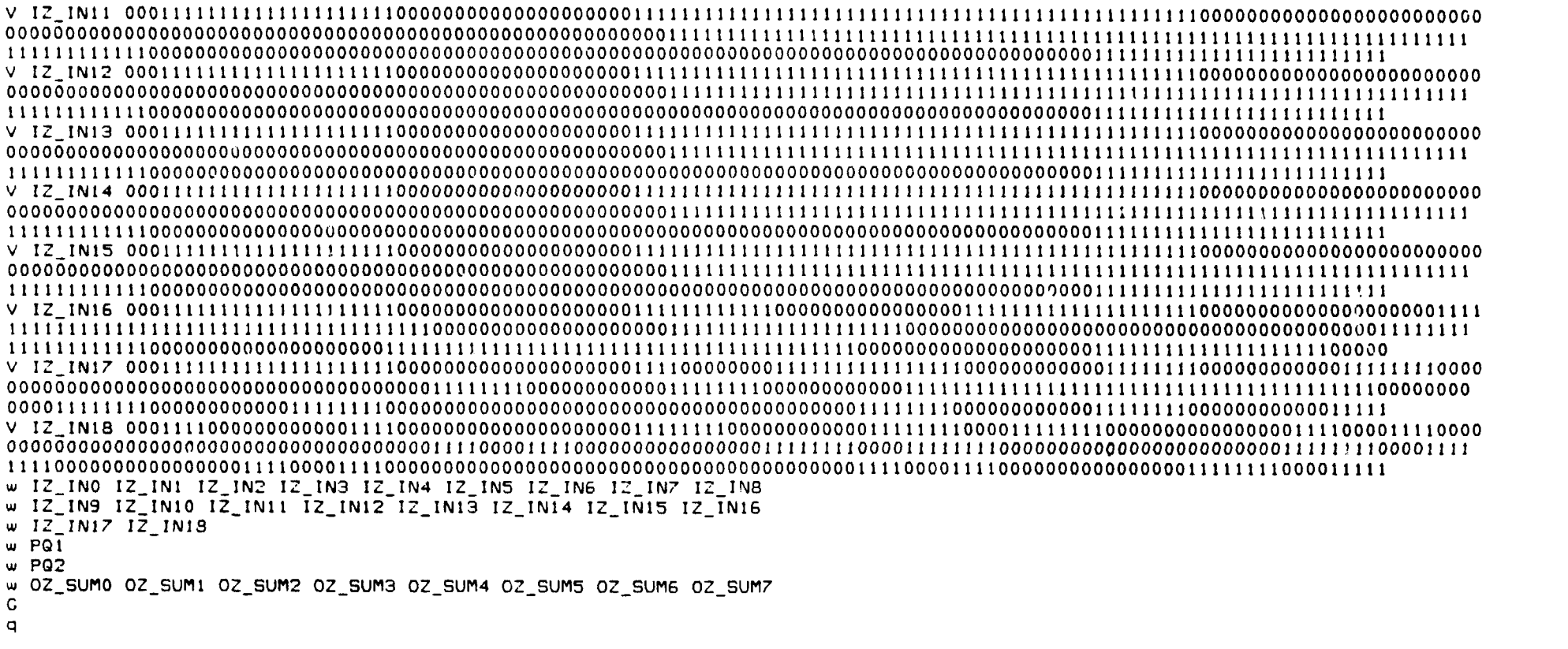

IZ_IN13
IZ_IN14
IZ_IN15
IZ_IN16
IZ_IN17
IZ_IN18
IZ_IN19
IZ_IN20
IZ_IN21
IZ_IN22
IZ_IN23
IZ_IN24
IZ_IN25
IZ_IN26
IZ_IN27

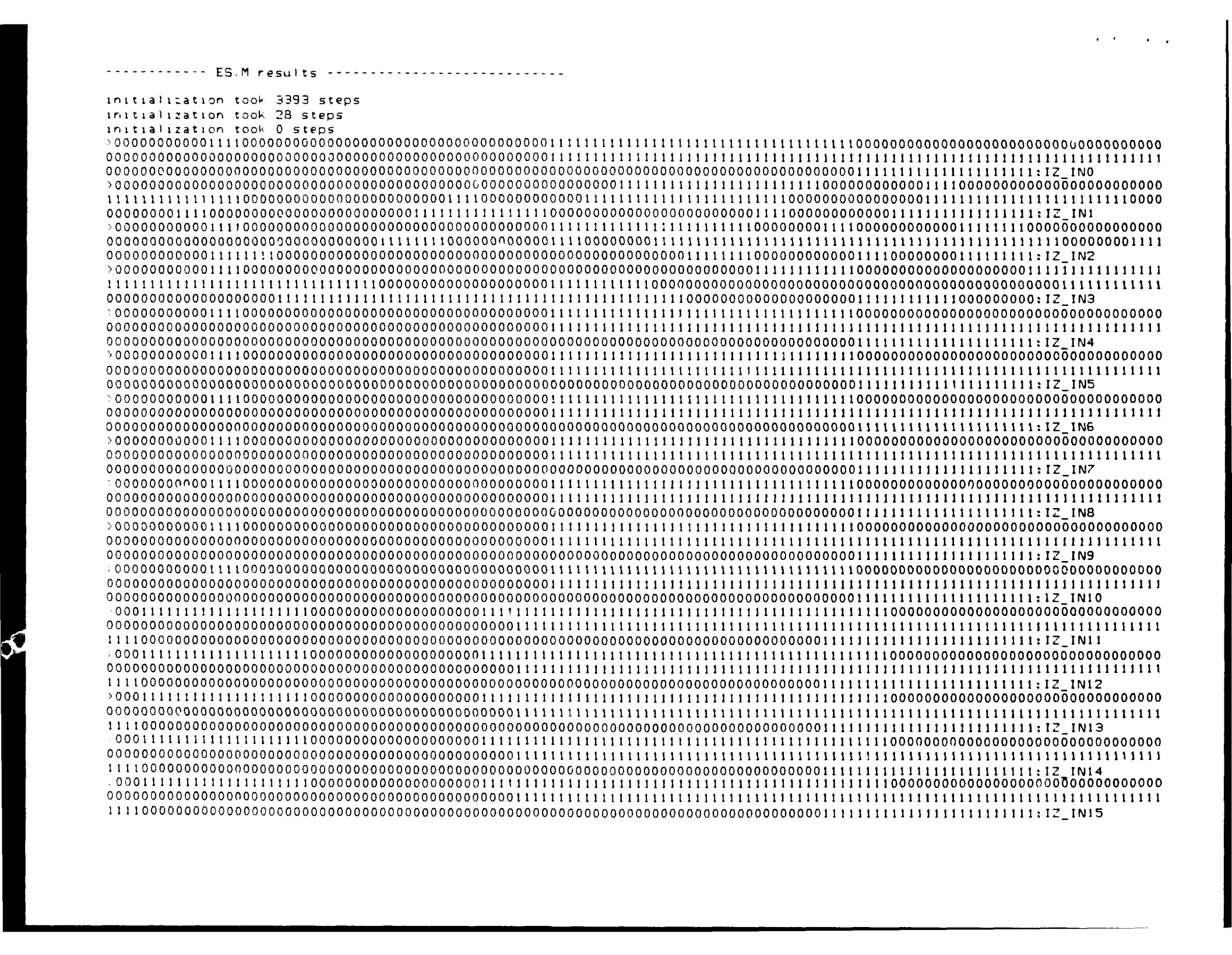

IZ_IN28
IZ_IN29
IZ_IN30
IZ_IN31
IZ_IN32
IZ_IN33
IZ_IN34
IZ_IN35
OZ_OUT0
OZ_OUT1
OZ_OUT2
OZ_OUT3
OZ_OUT4
OZ_OUT5
OZ_OUT6
OZ_OUT7
OZ_OUT8

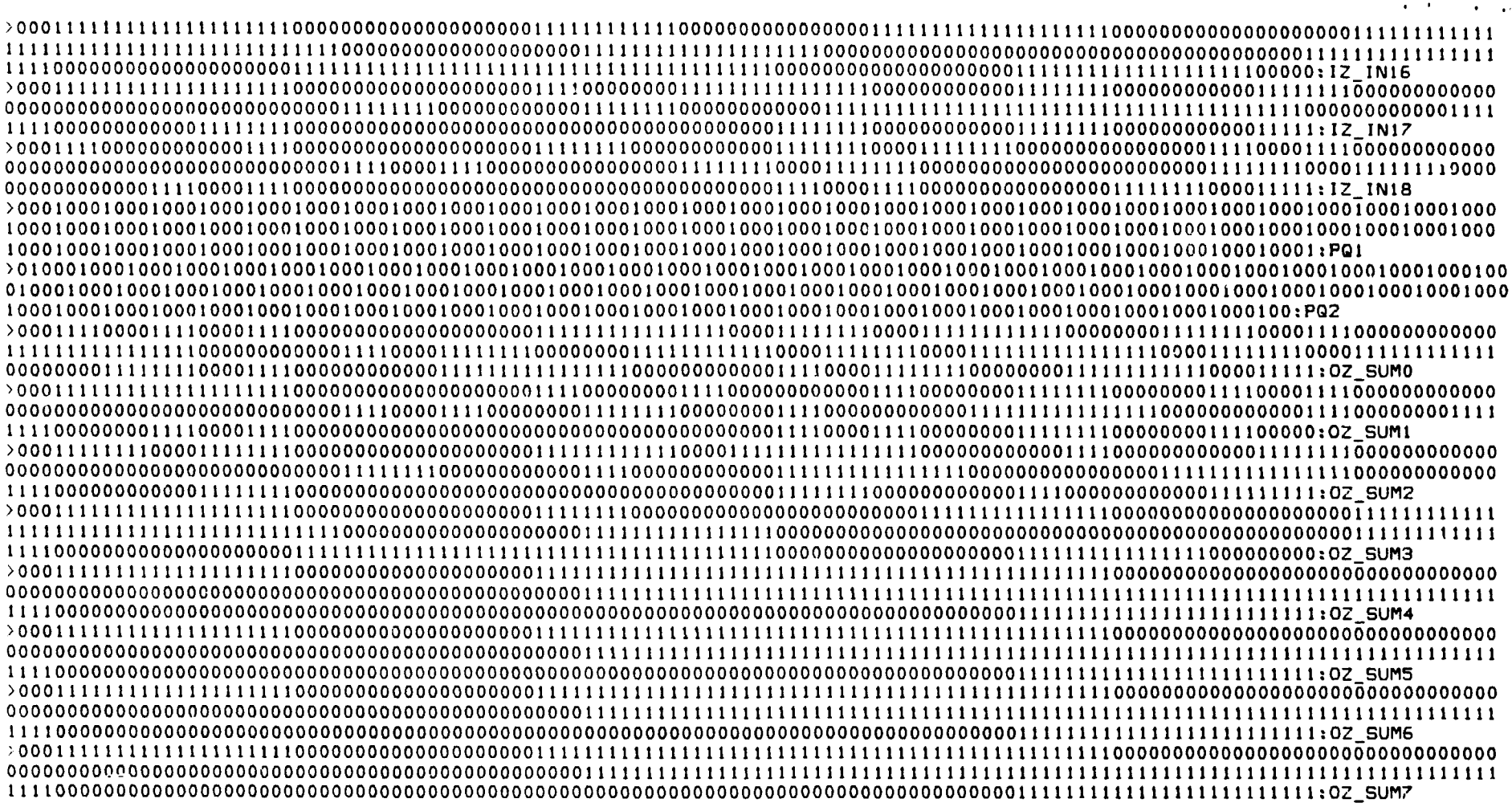

OZ_OUT9
OZ_OUT10
OZ_OUT11
OZ_OUT12
OZ_OUT13
OZ_OUT14
OZ_OUT15
OZ_OUT16
OZ_OUT17
OZ_OUT18
OZ_OUT19
OZ_OUT20
OZ_OUT21
OZ_OUT22
OZ_OUT23
OZ_OUT24


OZ_OUT25
OZ_OUT26
OZ_OUT27
OZ_OUT28
OZ_OUT29
OZ_OUT30
OZ_OUT31
OZ_OUT32
OZ_OUT33
OZ_OUT34
OZ_OUT35


h Vdd
l GND
l IZ_BUS_Select_1
l IZ_BUS_Select_2
l IZ_BUS_Select_3
h IZ_BUS_Select_4
V PQ2
V PQ1
V IZ_IN10
V IZ_IN9
V IZ_IN0
V IZ_IN1
V IZ_IN2
V IZ_IN3
V IZ_IN4
V IZ_IN5
V IZ_IN6
V IZ_IN7
V IZ_IN8


V IZ_IN11
V IZ_IN12
V IZ_IN13
V IZ_IN14
V IZ_IN15
V IZ_IN16
V IZ_IN17
V IZ_IN18
w IZ_IN0 IZ_IN1 IZ_IN2 IZ_IN3 IZ_IN4 IZ_IN5 IZ_IN6 IZ_IN7 IZ_IN8
w IZ_IN9 IZ_IN10 IZ_IN11 IZ_IN12 IZ_IN13 IZ_IN14 IZ_IN15 IZ_IN16
w IZ_IN17 IZ_IN18
w PQ1
w PQ2
w OZ_SUM0 OZ_SUM1 OZ_SUM2 OZ_SUM3 OZ_SUM4 OZ_SUM5 OZ_SUM6 OZ_SUM7
C
q


---------- ESM results ----------
initialization took 3393 steps
initialization took 28 steps
initialization took 0 steps
:IZ_IN0
:IZ_IN1
:IZ_IN2
:IZ_IN3
:IZ_IN4
:IZ_IN5
:IZ_IN6
:IZ_IN7
:IZ_IN8
:IZ_IN9
:IZ_IN10
:IZ_IN11
:IZ_IN12
:IZ_IN13
:IZ_IN14
:IZ_IN15


IZ_IN16
IZ_IN17
IZ_IN18
PQ1
PQ2
OZ_SUM0
OZ_SUM1
OZ_SUM2
OZ_SUM3
OZ_SUM4
OZ_SUM5
OZ_SUM6
OZ_SUM7

Appendix B — Cleaning Procedures

Consumables:

Sulfuric Acid , H_2SO_4

Hydrogen Peroxide, H_2O_2

Deionized Water (DIW)

Nitrogen gas, N_2

Equipment:

Pyrex/Glass Vessel (1 liter Beaker)

Polypropylene Wafer Holder

Nitrogen Spray Gun

Resistivity Measurement Device (for DIW)

Cleaning Process:

Step 1. Arrange the wafers in the wafer holder and make sure that the wafers can be totally submerged when placed in the beaker.

Step 2. In the beaker, mix the sulfuric acid and the hydrogen peroxide in the proportion of 3:2 (H_2SO_4 : H_2O_2).

Step 3. Immediately immerse the wafers into the solution for fifteen (15) minutes. The solution will bubble and remove organic contaminants from the wafer's surface.

Step 4. Remove the wafers from the solution and rinse in DIW until 5 MΩ purity is attained. This will take approximately five minutes if the wafers are rinsed well before being placed in a bath of continuously flowing DIW.

Appendix C — Oxidation (SiO_2) Procedures

Consumables:

Oxygen gas, O_2

Nitrogen gas, N_2

Deionized Water, DIW

Equipment:

Thermal Oxidation Furnace

Bubbler (for Thermal Oxidation Furnace)

Quartz wafer boat

Oxidation Process:

Step 1. The wafers were cleaned and dried in accordance with the cleaning procedures discussed in Appendix B.

Step 2. Ensure that the furnace is stable at $1050^{o}C$ at the center of the oxidation tube (zone 2).

Step 3. Load The wafers into the quartz boat.

Step 4. Begin O_2 flow in the tube and maintain the flow at approximately 1.0 l/min.

Step 5. Push the wafers slowly (2-3 cm/min) into the furnace until all wafers of the boat are in the hot zone. (Approx 30 cm down the length of tube.)

Step 6. Quickly slide the boat into the center of zone 2. (The center of the tube).

Step 7. After the O_2 has been flowing for 15 minutes, ensure that the bubbler is filled with DIW, and activate the O_2 flow through the bubbler to deliver steam to the tube. The open end of the tube can be checked to verify steam flow by positioning a cold (room temperature) mirror in the vent stream. If condensation forms, steam can be assured to be flowing in the tube.

Step 8. Monitor bubbler periodically to maintain the DIW level. Generate steam until the desired thickness of oxide is obtained. Using the standard graphs of oxide thickness versus time under steam conditions predicts approximately 20 hours are required for protection layer oxide. [14:50]

Step 9. Stop the steam flow and continue a dry O_2 flow for 15 minutes.

Step 10. (Reverse step 5) - Quickly pull the wafer boat through the oxidation tube to the edge of zone 2. Slowly (2-3 cm/min) pull the wafer boat out into zone 1, and then remove them from the oxidation tube. Allow the wafers to cool to room temperature.

Appendix D Photolithography Processes

Consumables:

Rubylith

Shipley 111s Positive Photoresist

Kodak High Resolution Photoplates (HRP)

Kodak HRP Developer

Acetic Acid Stop Bath

Fixing Solution

Methyl Alcohol

Versatec Plotter Film (40"wide)

Equipment:

Karl Suss MJB-UV300 Mask Aligner

Coordinatograph & Light Table

Camera (3" Lens)

PhotoPlate Duplicating Machine

PhotoPlate Holder

HRP Mask Making Process using Rubylith

Step 1. Using the MAGIC CAD tool, a file is created that contains the desired image.

Step 2. Write the file out in the Caltech Intermediate Form (CIF) format. Using the dimensions in that file, convert all values to mils (or inches). Multiply that number by the magnification that will be used to reduce it by the camera. (for example, 25x).

Step 3. Cut a sheet of Rubylith to the required size and secure it to the coordinatograph light table. Using a knife blade, cut the rectangles into the Rubilith as defined by the measurements obtained in part 2, and the coordinates displayed on the display tubes.

Step 4. Carefully remove the red Rubylith from the clear mylar backing in those areas which are to be clear (that is, pass light).

Step 5. Place the pattern on the light board in front of the camera.

Step 6. Align the camera according the predefined distance for the front and rear bellows for the magnification required.

Step 7. Using a magnifying device and a used HRP, visually focus the camera through the rear view hole so that the used plate emulsion side and the image are in focus at the same time. This may require movement of the camera bellows slightly. Now remove the used plate and under safelight conditions replace the plate holder in the camera.

Step 8. Expose the HRPfor the required time. The Rubylith images generally required a 2 minute exposure, but exposure time varied from 1 to 2 minutes depending on the age of the plates, contrast ratio of the image, and freshness of the developer.

Step 9. Under safelight conditions, remove the HRP from the camera holder, and place it in the development holder.

Step 10. Immerse the HRP in developer for five minutes, and provide constant agitation.

Step 11. Immerse the HRP in the stop bath solution for 30 seconds.

Step 12. Immerse the HRP in the fixer solution for 30 seconds.

Step 13. Rinse the HRPin DIW for 5 minutes or until 10 MΩ purity is obtained; rinse the HRP in methyl alcohol and dry with N_2.

HRP Plate Processing with Versatec Plotter Film

Step 1. Generate an image file as discussed in step 1. above.

Step 2. Write the output file in Calma GDS II form instead of the CIF format.

Step 3. Bring a tape of the binary file (GDS II) to the Avionics Laboratory CAD Facility and import the file to the Calma system. Convert the file and plot it on the Versatec flatbed plotter on Versatec film.

Step 4. Use the Versatec film in place of the Rubylith in the process steps 5-13 discussed above.

Wafer Alignment and Exposure

Step 1. Turn on the N_2 supply to the Mask Aligner.

Step 2. Turn-on the vacuum and load the mask into the holder.

Step 3. Turn-on the lamp power supply.

Step 4. When the display shows 'RDY', press the 'Start' Button.

Step 5. Turn-on the Aligner and the N_2 and Air switches to the aligner.

Step 6. Verify that the settings match the posted limits.

Step 7. Insert a photoresist coated wafer on the stage of the aligner.

Step 8. Using the lever on the left side of the aligner, make contact with the mask. If contact is not desired during exposure, the dial on the front of the aligner may be set to establish a separation between the wafer and mask. (If the aligner is equipped with a contact by-pass switch, then depress the switch and use the lever on the left to make the separation.) The dial was set to give a 2μm separation for the via pattern.

Proceed to step 13 for all except the first-level via mask.

Step 9. The IC die must have their alignment checked. Align the first die and attempt to align the others without breaking contact with the other die bond pads. If this is unsuccessful realign the first die; if successful proceed to step 13, otherwise, continue this step. Set the x-y coordinate, and rotation controls to zero.

Step 10. Move the wafer until the next die is in alignment. Take the readings from the x-y coordinate, and rotation axes. These represent the deviation of the second die.

Step 11. Repeat step ten for each die.

Step 12. Modify the original files to accommodate the misaligned die and repeat the procedure for all masks.

Step 13. Set the exposure time on the timer. (40 seconds for Polyimide, 2-3 minutes for 111s photoresist).

Step 14. Make the exposure, bring the wafer out of the aligner by making contact, and move the lever on the left side to release the wafer.

Step 15. Develop - Resist 312:DIW (1:1), Until the pattern is cleared. Develop the polyimide as described in Appendix H.

Step 19. Shut down the mask aligner by turning-off the lamp, turning-off the N_2 and Air to the aligner stage, remove the mask, shut-down the vacuum. Do not shut-down the N_2 to the Lamp Housing until the lamp has cooled (15 minutes).

Appendix E — Silicon Etch Procedures

Consumables:

Nitric Acid, HNO_3

Acetic Acid, CH_3COOH

Hydrofluoric Acid, HF

Nitrogen gas, N_2

Deionized Water, DIW

Pottasium Hydroxide, KOH

Isopropyl Alcohol

Equipment:

1 liter Teflon® beaker

Polypropylene wafer holder

Micrometer (or similar measuring device)

Granite block or polished plat surface

Scale or Balance (accurate to 0.1 g.)

Recirculating water bath

Planar Silicon Etch Process:

Step 1. In 1.0 liter beaker, mix 80 ml HF, 600 ml HNO_3, and 200 ml CH_3COOH . Allow 3 hours for the solution to stabilize before using.

Step 2. Clean the wafers in accordance with the standard clean procedures of Appendix B.

Step 3. Place the cleaned wafers in the solution from step 1.

Step 4. Periodically (5 min intervals) remove the wafers, Rinse in DIW for 1 minute. Dry with N_2 and measure the thickness of a control wafer using a micrometer or similar measuring device on a flat surface (polished granite block). Repeat this step until the wafer has reached the desired thickness.

Step 6. Rinse the wafers in DIW until the 10 MΩ Standard has been obtained.

Step 7. Dry the waferers with N_2.

Anisotropic Etch Process:

Step 1. Measure 750 mililiters of DIW and pour into a 1 liter container.

Step 2. Measure 304.7 grams of KOH and slowly mix into the DIW.

Step 3. Measure 18.7 grams of isopropyl alcohol and pour in the same container.

Step 4. Arrange wafers to be etched in the polyproylene boat and submerge in the KOH etchant.

Step 5. Place the container in a water bath at 70°C for 13-14 hours. Periodically, visually inspect the wafers to determine if the windows have etched through the Si wafers.

Step 6. When all windows are completely clear, remove from etchant and rinse in DIW until the 10MΩ standard has been obtained.

Step 7. Dry the wafers with N_2.

Appendix F — Die Processing

Consumables:

Silicon wafer with die holes

VLSI circuit die

Acetone

Master Bond EP3CA (Special) Epoxy

Cotton swabs

Equipment:

Hot Plate (175^{o}C)

Glass plate (Cleaned HRP Substrate)

Tweezers

Epoxy Process:

Step 1. Mix epoxy 5 grams of part B,and 10grams of part A.

Step 2. Place the wafer face down on the HRP substrate.

Step 3. With tweezers, position an IC die in an opened window in the Si substrate in the face down position.

Step 4. While applying force to the die, apply epoxy around the perimeter of the die.

Step 5. Apply weights to the back surface of the substrate to maintain pressure on the die and the wafer to afford little chance for epoxy to seep onto wafer's surface (which is down).

Step 6. Heat the combination on a hot plate at 50°C for 15 minutes. Periodically check the status of the epoxy on the surface. If desired, remove the die with acetone.

Step 7. Remove wafer from the heat source. Examine the viscous nature of the epoxy. If the epoxy sags then return it to the heat source. Otherwise follow the topological measurements detailed in Appendix G.

Step 8. If the topology of the wafer is within -1 micron limit of planarity return it to the heat source and increase the temperature to 175°C for 1 hour. Examine as needed to check the epoxy cure.

Step 9. If the wafer and die transition is not planar, apply force to the die until it protrudes slightly from the front of the wafer. Using pressure from the back-side press the wafer and IC die combination onto the planar surface to level the die. Repeat until the transition is planar.

Step 10. Repeat steps 1-9 for other IC die.

Step 11. When the wafer has three IC die in the substrate, place in an oven for a high temperature cure (250°C) for 1 hour.

Step 12. After the IC dice are completely bonded into the substrate, place the epoxy on the back of both the dice and the wafer and bond this sub-assembly to the support wafer. The wafer epoxycure process is now complete.

Appendix G — Surface Topology Measurement

Consumables:

None

Equipment Used:

Sloan Dektak II A, Profile Measurement System

Wafer with mounted IC die

Process:

Step 1. The wafer is placed on the bed of the profilometer. If the wafer is in the epoxy cure stage, it is placed onto two glass slides that act as a carrier to prevent the epoxy from touching any other surface.

Step 2. The profilometer is then set-up with the proper variables for the measurement by selecting the program key. The parameters used for the epoxy measurement are: Scan Speed = low, Scan Length = 1 mm, and the profile varied (Depending on the initial plot result).

Step 3. The wafer is then positioned so that the probe will not damage the surface features, but so it will touch the die only as far as the edge of the ring. The interior of the die is somewhat protected by the overglass layer, but to avoid the possibility of damage, the interior of the IC die mounted in the wafer are not probed with the profilometer.

Step 4. The scan button is depressed and the output is viewed. If adjustments are required, then steps 2-4 are repeated until a scan graph appears that covers the area of the

die-to-wafer interface region. The cursors (Top, Bottom, R and M) may be positioned around the graph until the area of interest is displayed. The graph is then printed on the attached printer.

Appendix H — Dielectric Application Processing

Consumables:

Selectilux HTR 3-200 Polyimide

Selectiplast AP-1 Adhesion promoter

Selectiplast D-2 Developer

Isopropyl Alcohol

Deionized Water, DIW

Equipment:

Photoresist spinner

Photomasks (4 inch x 4 inch square Kodak High Resolution Plates, HRP)

Karl Suss MJB-UV300 Mask Aligner

Convection Oven

Hot Plate

Glass Beaker

Dielectric Processing:

Step 1. The adhesion promoter is mixed in a glass beaker. The following chemicals are added to the beaker and then stirred: isopropyl alcohol (95 ml), AP-1 (1-15 ml), DIW (5 ml).

Step 2. The wafer is baked in the oven for 30 minutes at 150^{o}C to drive-off the moisture.

Step 3. The wafer is placed on the spinner and a dropper of adhesion promoter is deposited onto the surface and allowed to cover the wafer.

Step 4. The wafer is spun at 4000 RPM for 30 seconds to spread the adhesion promoter evenly across the wafer's surface.

Step 5. The wafer is placed on a hot plate for 60 seconds at 150°C to dry the AP-1.

Step 6. The wafer is put back on the spinner and covered with polyimide near the center of the wafer. The polyimide is allowed to flow to fill-in the gaps in coverage and then it is spun at 1000 RPM for 20 seconds to obtain a uniform film whose thickness is greater than or equal to 10μm after cure.

Step 7. The wafer is then softbaked at 65°C for two hours to harden the emulsion.

Step 8. The wafer is aligned to the pattern and exposed on the mask aligner whose exposure energy density is greater than 400 mJ/cm^2. (10 mW/cm^2 for 40 s).

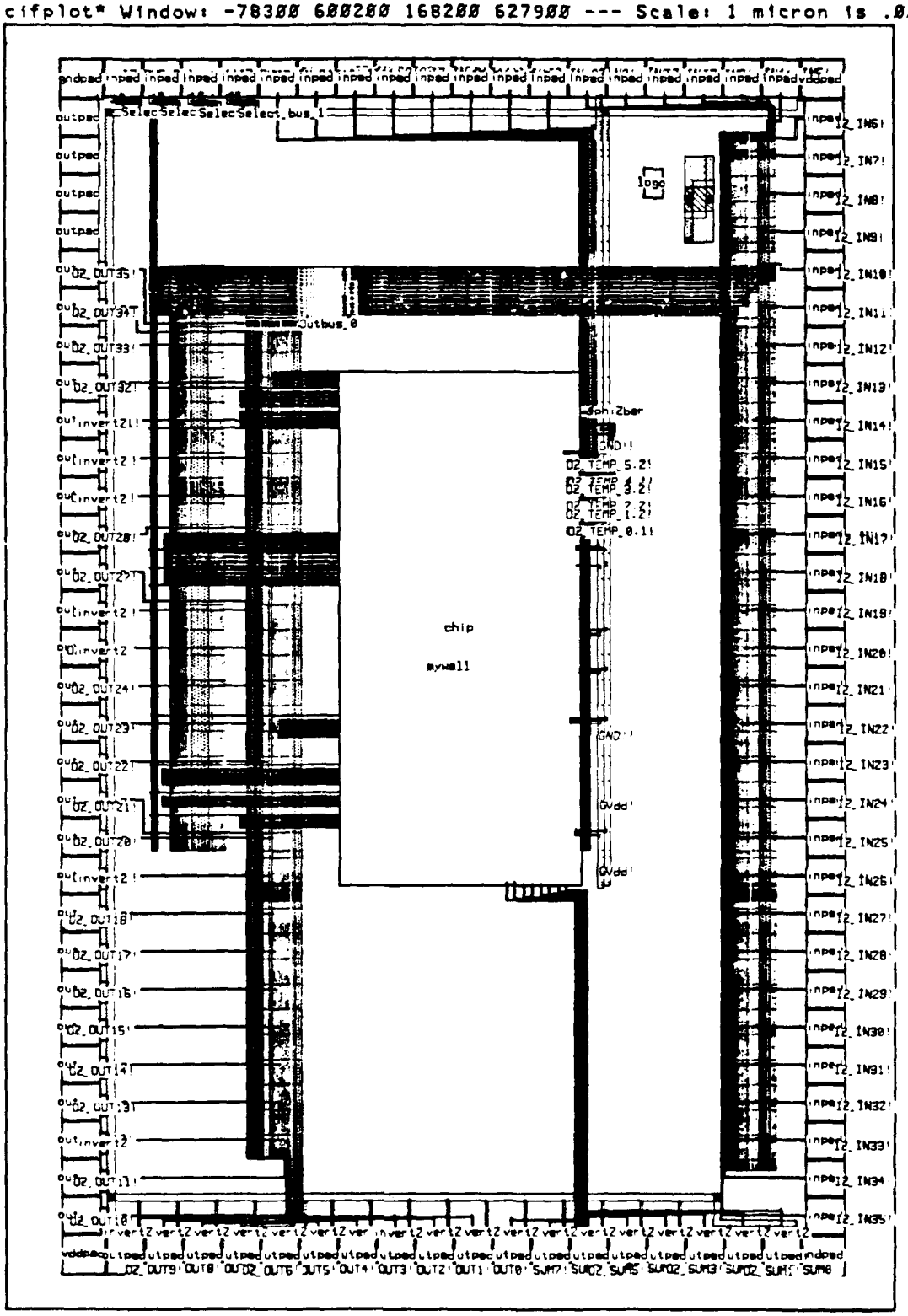
Step 9. Place the wafer on the spinner and develop it for 20 seconds at 500 RPM. Rinse it with isopropyl alcohol and dry with N_2.

Appendix I — Hilbert Transform Chip CIF Plots

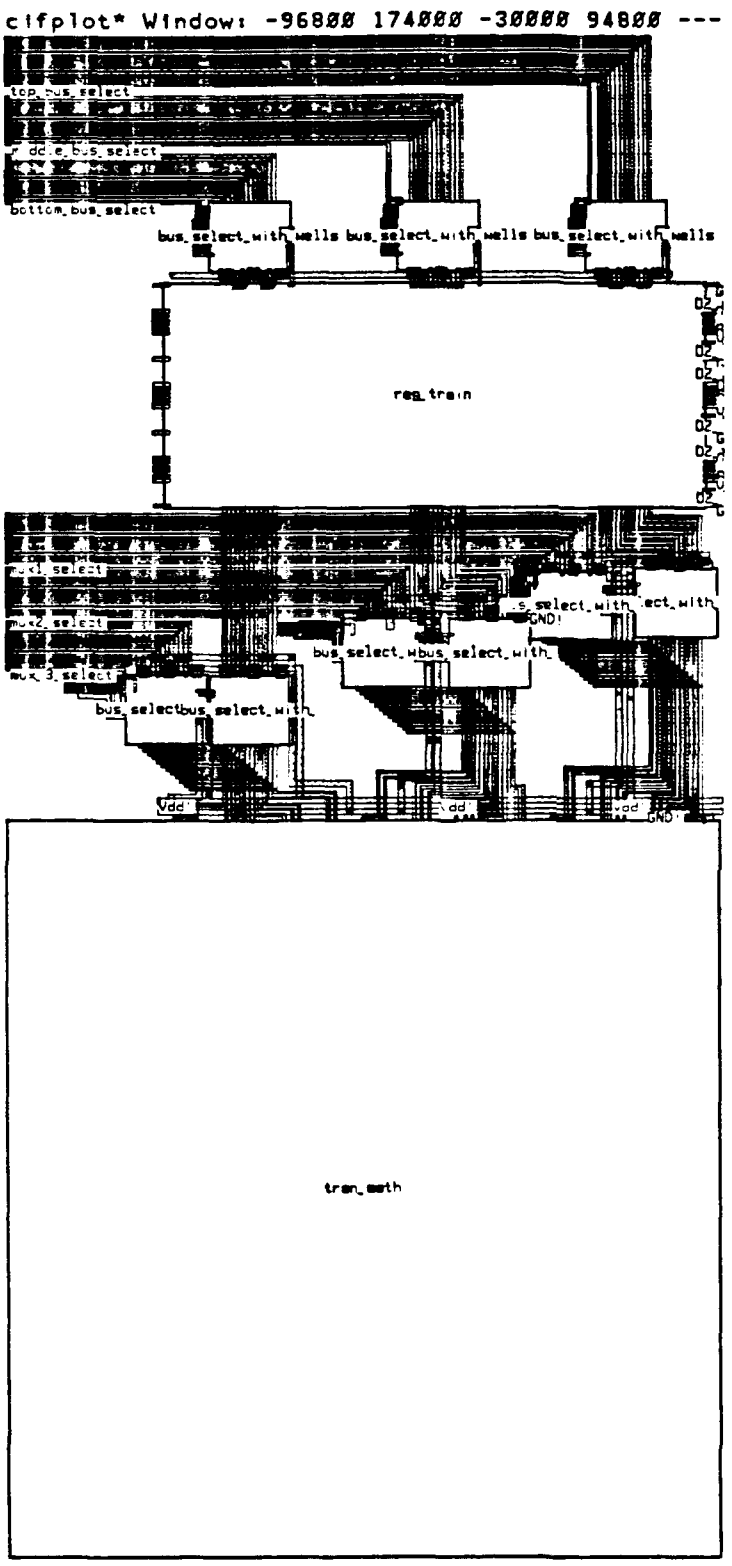
CIF PLOTS

This appendix shows the IC layout of the Hilbert transform fabricated for this investigation. The plots are shown in the Caltech Intermediate Format as plotted on the Versatec plotter by the CIFPLOT program. (The circuit will be plotted in overview and then individual portions will be presented).

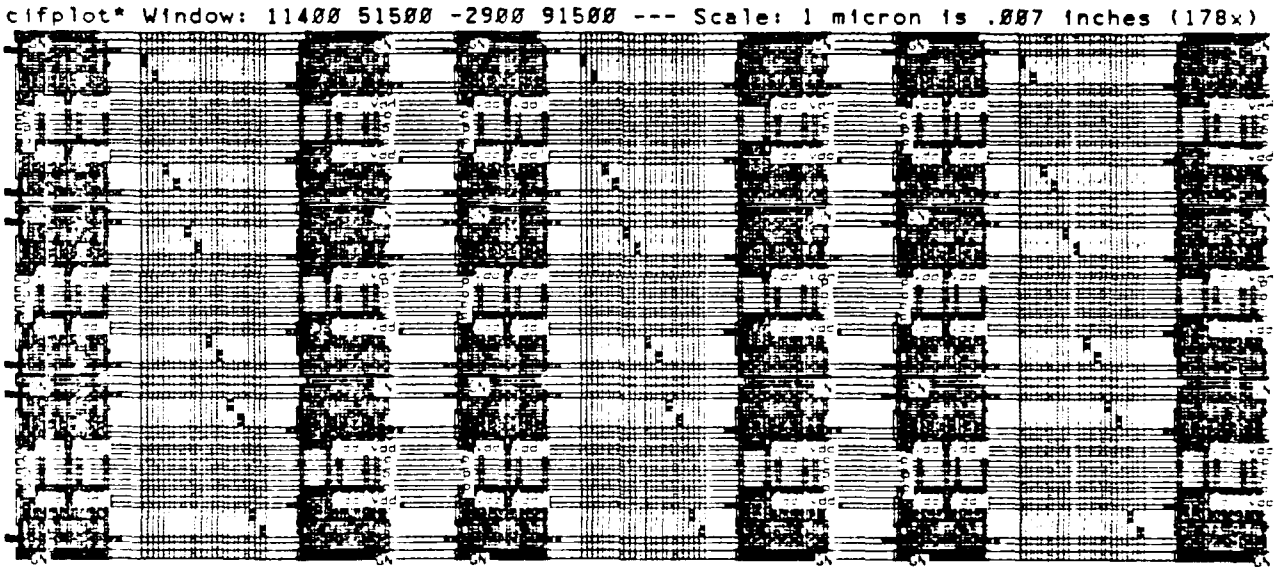
cifplot* Window: -78300 600200 168200 627900 --- Scale: 1 micron is .0012 inches (30x)



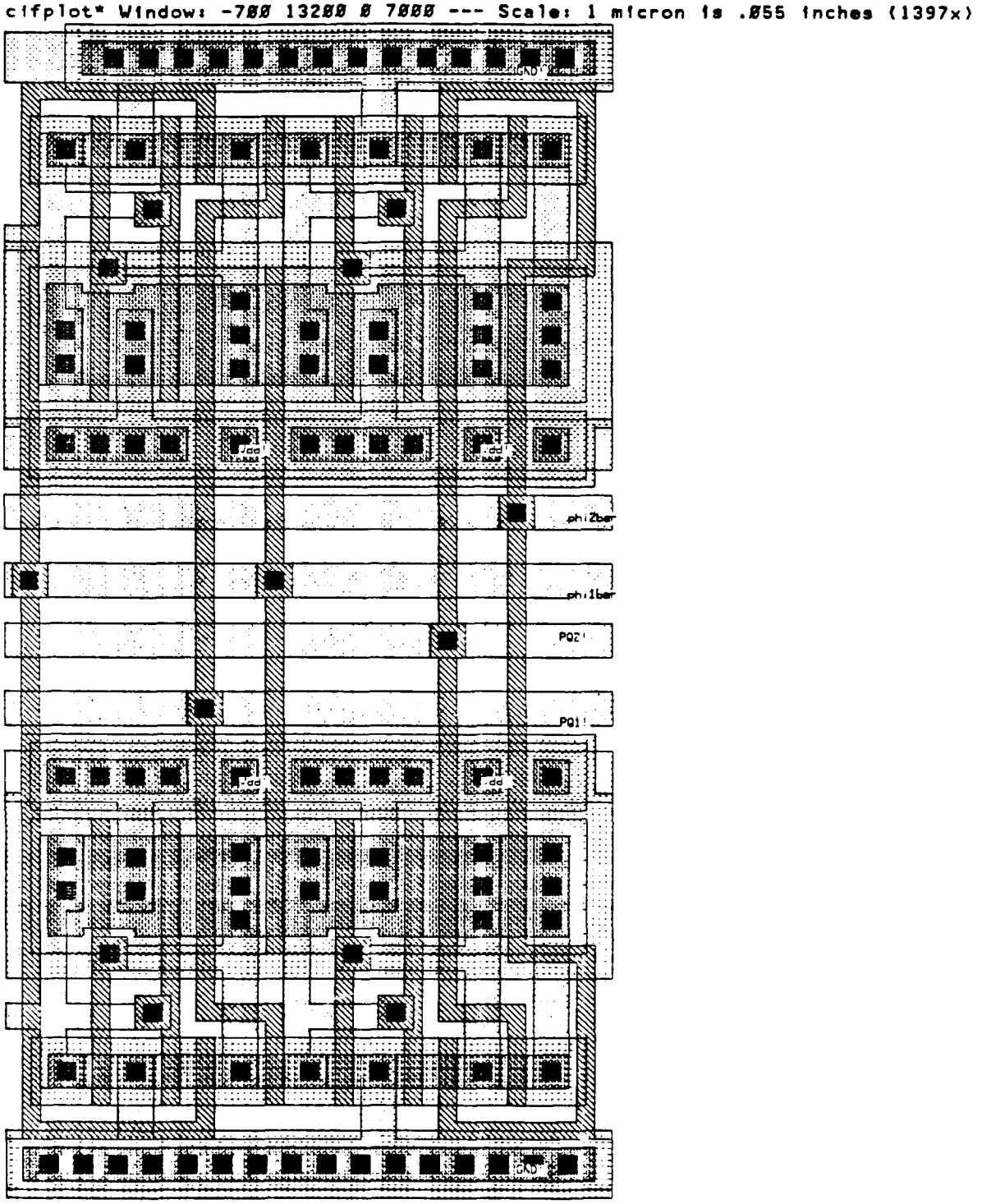
The full VSLI Circuit of The Hilbert Transform



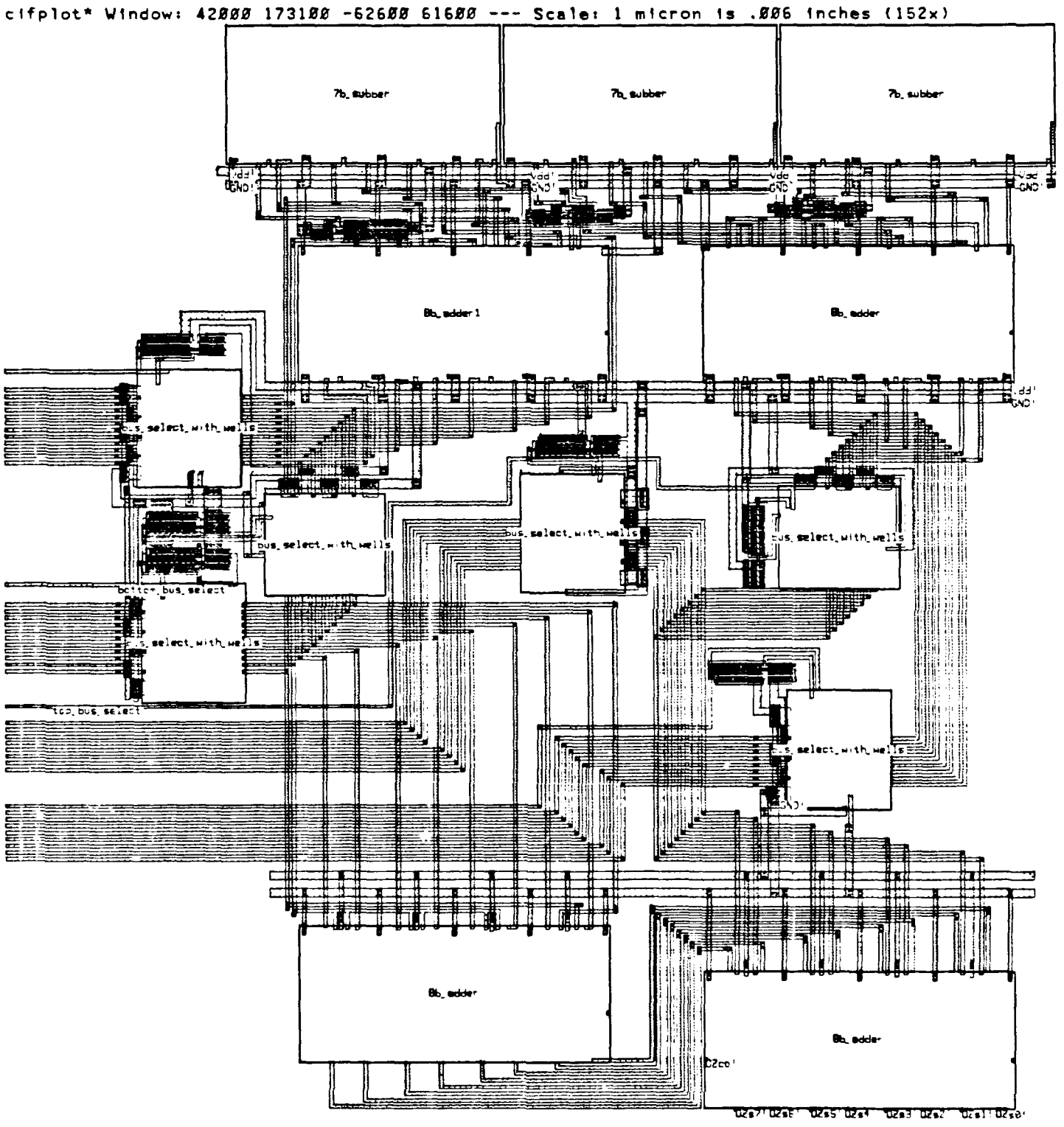
The Chip, showing the Register Train and the Tran_Math Sections



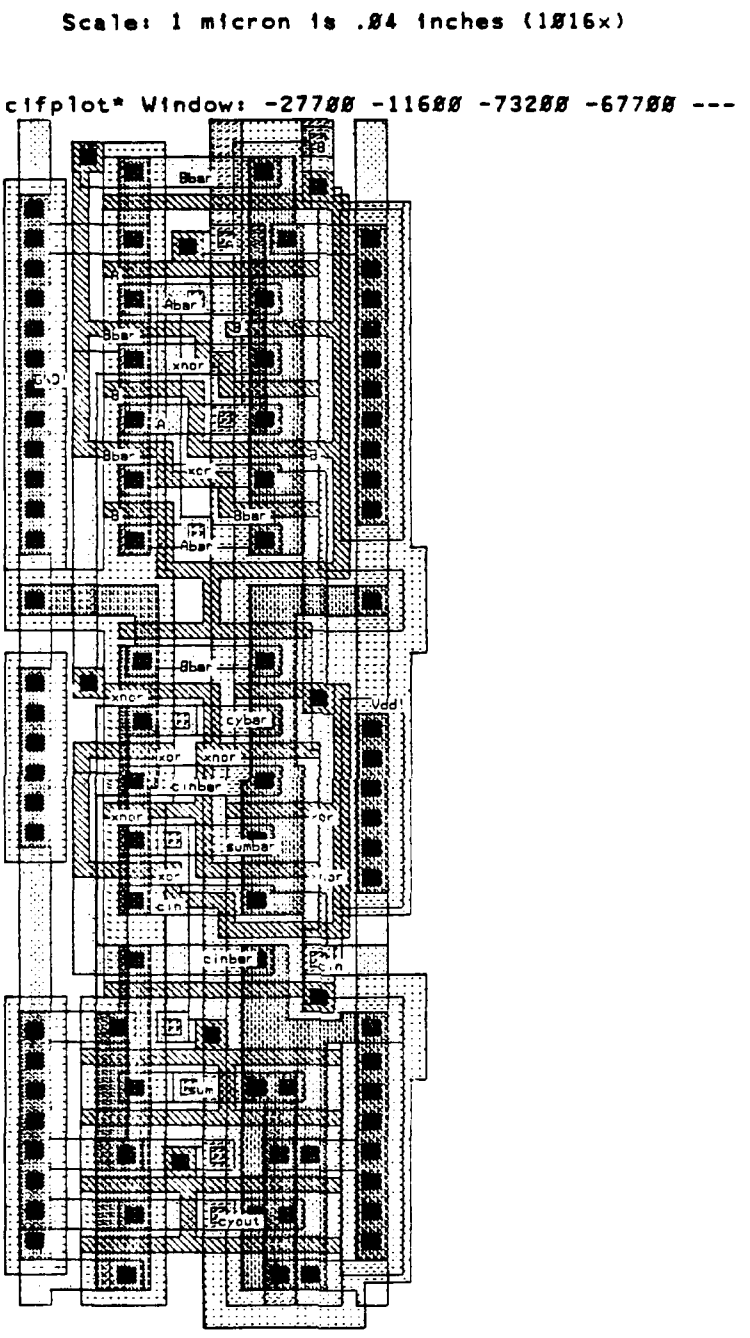
The Register Train section, showing the individual registers



Detailed View of the two-bit Register



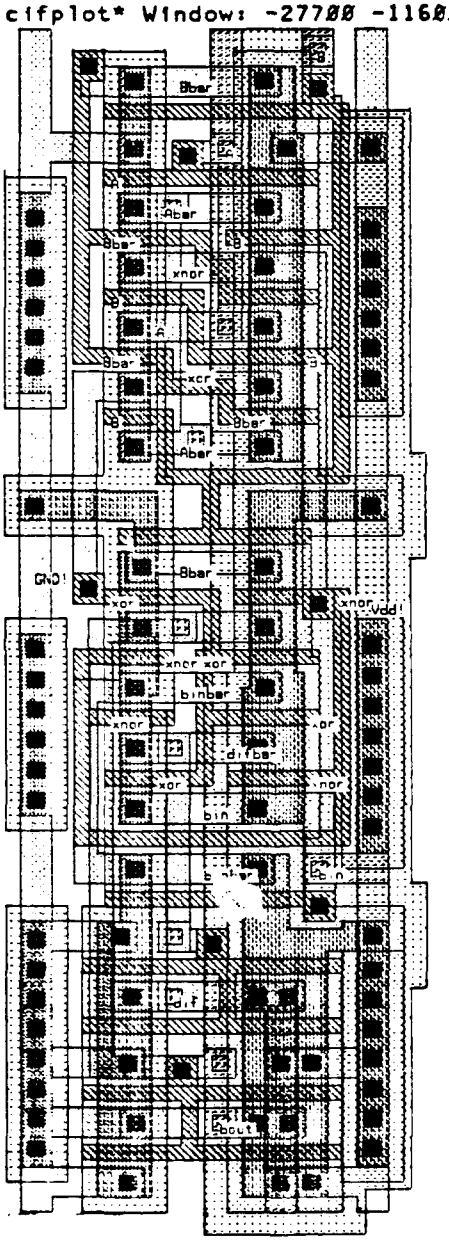
The Tran_Math Section of the circuit



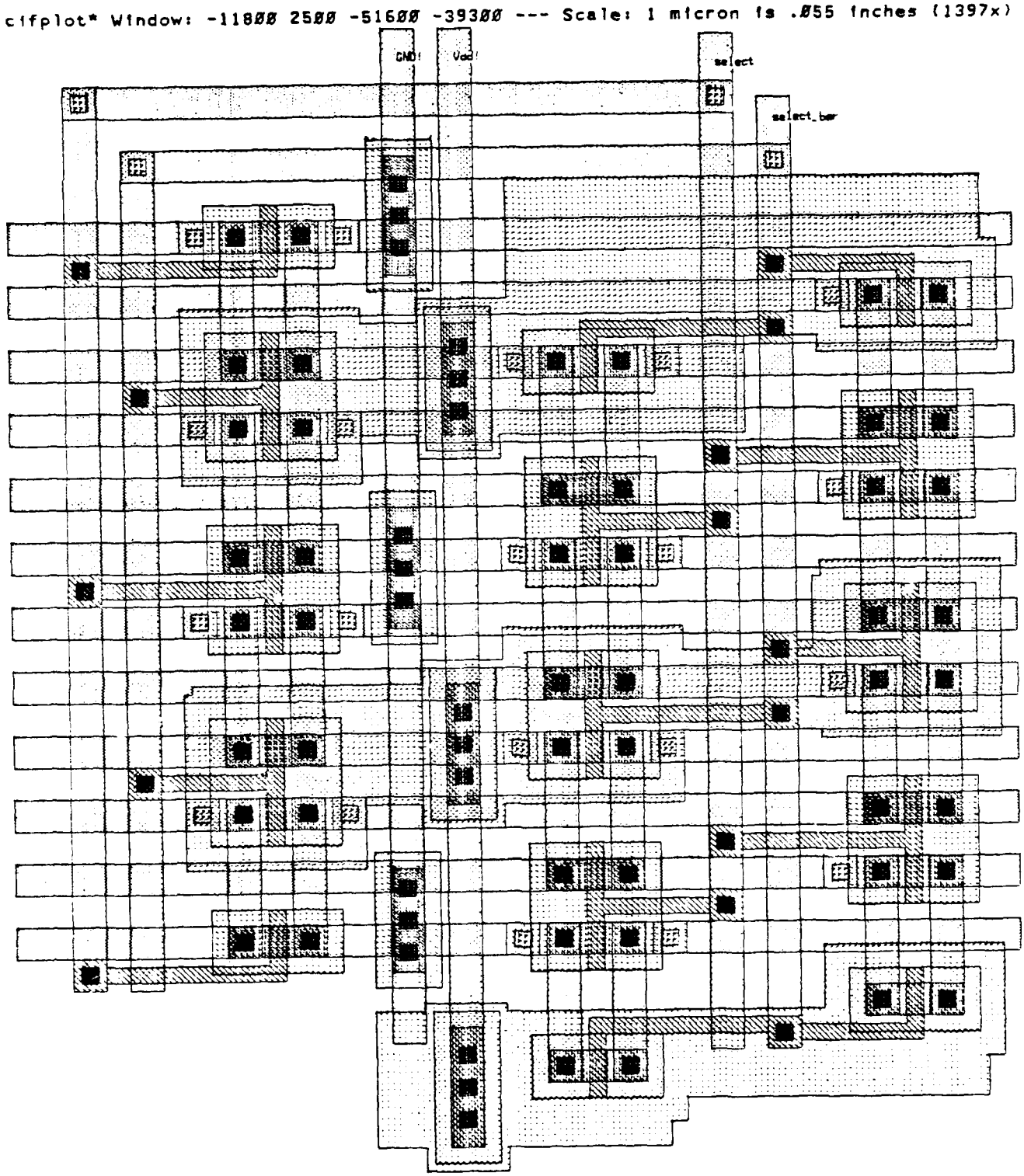
The Adders used in the Tran_Math Section of the circuit

Scale: 1 micron is .04 inches (1016x)

cifplot* Window: -27700 -11600 -66800 -61300 ---



The Subtractors used in the Tran_Math Section of the circuit



The Bus_Select T-Gate array used for off chip sampling

Bibliography

1. Takahashi, Lt. G. L. *Fabrication and Electrical Characterization of Multilevel Aluminum Interconnects Used to Achieve Silicon-Hybrid Wafer-Scale Integration*. MS Thesis, AFIT/GE/ENG/87D-65. Department of Electrical Engineering, Air Force Institute of Technology (AU), Wright Patterson AFB OH, December 1987.

2. Balde, John W., and Segelken, *1988 Electronics Components Conference*. 1988.

3. Brewer, Joe and Michael J. Little. Eds. *1990 Proceedings International Conference on Wafer Scale Integration*. vii. Washington: IEEE Computer Press, 1990.

4. Chakravorty, K. K. and others. "Hybrid Wafer Scale Integration Using Photosensitive Polyimide Dielectric and Electroplated copper Conductor Lines," *3rd International SAMPE Electronics Conference*. 1213-1223 1989.

5. Johnson, R. W. and others "Silicon Hybrid Wafer-Scale Package Technology," *IEEE Journal of Solid State Circuits*. *SC-21*:845-851 (October 1986).

6. ——. " Multichip Thin Film Technology on Silicon," *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*. *12*:185-194 (June 1989).

7. Mcdonald, J. F. and others "Techniques for Fabrication of Wafer Scale Interconnections in Multi-Ship Packages," *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*. *12*:195-205 (June 1989).

8. Hagge, J. K. "Ultra-Reliable Packaging for Silicon-on-Silicon WSI," *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*. *12*:170-179 (June 1989).

9. Chao, C. C. and others. "Multi-Layer Thin-Film Substrates for Multi-Chip Packaging," *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*. *12*:180-184 (June 1989).

10. Bassous, Ernest. "Fabrication of Novel Three-Dimensional Microstructures by the Anisotropic Etching of (100) and (110) Silicon," *IEEE Transactions on Electronic Devices*, *25*:1178-1192 (October 1978).

11. Brenner, Walter, Personal Correspondence, Technical Development, Master Bond, Inc. Teaneck, N.J. Jun-July 1990.

12. *Teflon® Products for Research and Industry*, Product Catalog, Berghof/America Inc., Undated.

13. Sze, S. M. *Physics of Semiconductor Devices (Second Edition)*, New York: John Wiley & Sons, 1981.

VITA

Captain Daniel J. Gaughan [redacted]

[redacted] He graduated from Westfield High School in Westfield Massachusetts in 1979. He then went on to attend Norwich University where he earned a Bachelor of Science in Electrical Engineering in 1983. He was commissioned a Second Lieutenant in the Air Force in July of that year and was assigned to Aeronautical Systems Division at Wright-Patterson AFB OH. He served with the Directorate of Engineering there until he entered the School of Engineering at the Air Force Institute of Technology in May of 1989.

[redacted]

December 1990 Master's Thesis

Silicon Hybrid Wafer Scale Integration (WSI) Used to Fabricate a Hilbert Transform Integrated Circuit Module

Daniel J. Gaughan

Air Force Institute of Technology AFIT/GE/ENG/90D-22
Wright-Patterson AFB OH 45433-6583

Approved for Public Release;
Distribution Ulimited

This research was performed in order to develop a superior processing schedule for fabricating Wafer-Scale Integration (WSI) circuit modules. This technology allows the design of circuitry that spans the entire surface of a silicon substrate wafer. The circuit element employed in this research was the Hilbert transform, a digital phase-shifting circuit. The transform was incorporated into a three Integrated Circuit (IC) die package that consisted of a mechanically supportive silicon wafer, the three IC die, and a planarizing silicon wafer. The die were epoxied into this wafer using a Teflon block as a flat, and the combination was epoxied onto the substrate wafer, forming the IC module. The original design goals of this research were to keep the IC die and wafer planar and to electrically characterize the module's interconnects. The first goal was met; the resultant process uses a low temperature (50°C) cure to achieve die-to-wafer planarity of within 5 microns. The second was not met due to the inability to pattern the chosen photosensitive dielectric material. Recommendations for further research included the need to use a stable non-stick surface as a epoxy cure fixture and the need to investigate the photopatternable dielectric material.

Wafer Scale Integration, Wafer, Interconnects, Semiconductor, Integrated Circuit, Very Large Scale Integration 97

Unclassified Unclassified Unclassified UL

GENERAL INSTRUCTIONS FOR COMPLETING SF 298

The Report Documentation Page (RDP) is used in announcing and cataloging reports. It is important that this information be consistent with the rest of the report, particularly the cover and title page. Instructions for filling in each block of the form follow. It is important to **stay within the lines to meet optical scanning requirements.**

Block 1. Agency Use Only (Leave Blank)

Block 2. Report Date. Full publication date including day, month, and year, if available (e.g. 1 Jan 88). Must cite at least the year.

Block 3. Type of Report and Dates Covered. State whether report is interim, final, etc. If applicable, enter inclusive report dates (e.g. 10 Jun 87 - 30 Jun 88).

Block 4. Title and Subtitle. A title is taken from the part of the report that provides the most meaningful and complete information. When a report is prepared in more than one volume, repeat the primary title, add volume number, and include subtitle for the specific volume. On classified documents enter the title classification in parentheses.

Block 5. Funding Numbers. To include contract and grant numbers; may include program element number(s), project number(s), task number(s), and work unit number(s). Use the following labels:

C	- Contract	**PR**	- Project
G	- Grant	**TA**	- Task
PE	- Program Element	**WU**	- Work Unit Accession No.

Block 6. Author(s). Name(s) of person(s) responsible for writing the report, performing the research, or credited with the content of the report. If editor or compiler, this should follow the name(s).

Block 7. Performing Organization Name(s) and Address(es). Self-explanatory.

Block 8. Performing Organization Report Number. Enter the unique alphanumeric report number(s) assigned by the organization performing the report.

Block 9. Sponsoring/Monitoring Agency Names(s) and Address(es). Self-explanatory.

Block 10. Sponsoring/Monitoring Agency. Report Number. (If known)

Block 11. Supplementary Notes. Enter information not included elsewhere such as: Prepared in cooperation with...; Trans. of ..., To be published in .... When a report is revised, include a statement whether the new report supersedes or supplements the older report.

Block 12a. Distribution/Availablity Statement. Denote public availability or limitation. Cite any availability to the public. Enter additional limitations or special markings in all capitals (e.g. NOFORN, REL, ITAR)

DOD - See DoDD 5230.24, "Distribution Statements on Technical Documents."
DOE - See authorities
NASA - See Handbook NHB 2200.2.
NTIS - Leave blank.

Block 12b. Distribution Code.

DOD - DOD - Leave blank
DOE - DOE - Enter DOE distribution categories from the Standard Distribution for Unclassified Scientific and Technical Reports
NASA - NASA - Leave blank
NTIS - NTIS - Leave blank.

Block 13. Abstract. Include a brief (Maximum 200 words) factual summary of the most significant information contained in the report.

Block 14. Subject Terms. Keywords or phrases identifying major subjects in the report.

Block 15. Number of Pages. Enter the total number of pages.

Block 16. Price Code. Enter appropriate price code (NTIS only).

Blocks 17. - 19. Security Classifications. Self-explanatory. Enter U.S. Security Classification in accordance with U.S. Security Regulations (i.e., UNCLASSIFIED). If form contains classified information, stamp classification on the top and bottom of the page.

Block 20. Limitation of Abstract. This block must be completed to assign a limitation to the abstract. Enter either UL (unlimited) or SAR (same as report). An entry in this block is necessary if the abstract is to be limited. If blank, the abstract is assumed to be unlimited.